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**DESIGN, IMPLEMENTATION AND  
EVALUATION OF AN EMBEDDED  
ELECTRONIC SYSTEM FOR THE  
COTROL OF A TRANS-RADIAL  
PROSTHESIS**

Faculty of Engineering and Natural Sciences  
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# ABSTRACT

Nicolas Trimborn: Design, implementation and evaluation of an embedded electronic system for the control of a trans-radial prosthesis

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This thesis presents the design of an embedded electronic platform intended for use by students of the *CYBATHLON* project course offered at Technische Universität München (TUM) to develop an improved trans-radial prosthesis in the lead up to the *CYBATHLON 2024 Competition*. The design of the new platform was based on the analysis of limitations of the current electronics platform and the current state-of-the-art commercial and research prostheses. The necessary hardware and firmware was developed to operate the diverse hardware elements and facilitate tasks such as motor control, sensor feedback and real-time communication. The comprehensive electronics platform was then verified with the help of a test bench.

Three main improvements to the existing *CyberTUM* prosthesis were realised through this work. The newly developed electronics platform achieved a 290% reduction in electronics footprint from the previous platform, while still providing additional features and supporting four Brushless DC (BLDC) motors. The new design provides a high level of flexibility not previously possible. The defined expansion interfaces can be used to customise the supported functionality without affecting rest of the platform in order to minimise the effort required to support new features or future prosthesis configurations. Finally, the sensor implementation was improved and protection features were added to improve robustness. A fully functional prototype was created, assembled and tested and the required firmware was developed.

The design provisions made will enable future students to develop the next generation *CyberTUM* prosthesis. The improved electronic design capabilities will empower the team to tackle the challenges of the *CYBATHLON 2024 Competition*

Keywords: Trans-radial Prosthesis, EtherCAT, Brushless DC (BLDC), Six-step Commutation (6SC), Cascaded Control, EMG, ADS1299

The originality of this thesis has been checked using the Turnitin OriginalityCheck service.

# Design, Implementation and Evaluation of an Embedded Electronic System for the Control of a Trans-radial Prosthesis

Wissenschaftliche Arbeit zur Erlangung des Grades  
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# Anhang I

## Erklärung

Ich versichere hiermit, dass ich die von mir eingereichte Abschlussarbeit selbstständig verfasst und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.



15.11.2021

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Garching, Datum, Unterschrift

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# Abbreviations

6SC	Six-step Commutation.
ADC	Analog-to-digital converter.
ADL	Activites of daily living.
AFE	Analog front end.
ASIC	Application-specific integrated circuit.
BBH	Be-bionic Hand.
BGA	Ball Grid Array.
BLDC	Brushless DC.
CMRR	Common Mode Rejection Ratio.
DC	Direct Current.
DLRHAS	Deutsches Zentrum für Luft und Raumfahrt Hand Arm System.
DMA	Direct memory access.
DOA	Degree of Actuation.
DOF	Degrees of Freedom.
EDA	Electronic design automation.
EMG	Electromyography.
ESC	EtherCAT Slave Controller.
ESD	Electrostatic discharge.
ETH	Eidgenössische Technische Hochschule Zürich.
FOC	Field-oriented Control.
FPU	Floating-point unit.
FSR	Force-Sensing Resistor.
GPIO	General Purpose Input or Output.
HAL	Hardware Abstraction Layer.
HMI	Human Machine Interface.
IC	Integrated Circuit.
IMU	Inertial measurement unit.
MCB	Master Control Board.
MCU	Microcontroller Unit.
MIRMI	Munich Institute of Robotics and Machine Intelligence.
MOSFET	Metal-oxide-semiconductor field-effect transistor.
NiCd	Nickel-Cadmium battery.

NiMH	Nickel metal hydride battery.
OCP	Over Current Protection.
OTP	Over Temperature Protection.
OVP	Over Voltage Protection.
PCB	Printed Circuit Board.
PMSM	Permanent magnet synchronous motors.
PR	Pattern Recognition.
PWM	Pulse-width modulation.
QSPI	Quad Serial Peripheral Interface.
RCB	Reverse Current Blocking.
RPP	Reverse Polarity Protection.
SBC	Single Board Computer.
SCB	Slave Control Board.
SCP	Short Circuit Protection.
SEG	System Electric Greifer.
sEMG	Surface Electromyography.
SH-P	SoftHand Pro.
SH2-P	SoftHand 2 Pro.
SHAP	Southampton Hand Assessment.
SHS	Sensor Hand Speed.
SoSe	Summer Semester.
SPI	Serial Peripheral Interface.
TUM	Technische Universität München.
UVLO	Under-Voltage Lock Out.

# 1. Introduction

Throughout history, people who have lost limbs due to illness or injury have used increasingly sophisticated prostheses to replicate the function of their lost extremities. As of 2017, an estimated 57.7 million people worldwide are living with limb amputation, of which upper limb amputations make up over 38% (22.3M). Trans-radial (below the elbow) amputations account for up to 60% (13.4M) of the upper limb amputations [McD+21]. The versatility and dexterity of currently available prosthetic solutions is limited with respect to the number of tasks that can be successfully performed. Current state-of-the-art upper arm prostheses still struggle with tasks performed in every day living. As such, the need for innovative prosthesis research to improve current solutions is significant.

## 1.1. Motivation

The *CYBATHLON* is an innovation challenge organised by [Eidgenössische Technische Hochschule Zürich \(ETH\)](#) aimed at fostering the development of assistive technologies for people with disabilities. The associated research and development efforts of participating teams is motivated and displayed in a competition format. The spectrum of assistance systems addressed by the competition include powered arm, leg, exoskeleton and wheelchair solutions, among others. Most current assistive devices lack satisfactory function, which limits the acceptance and retention amongst prosthesis users. The competition aims to promote research to improve the assistive technologies while also improving the communication between developers and people with disabilities.

The [Technische Universität München \(TUM\)](#) *CYBATHLON* team participated in the 2020 powered arm prosthesis competition by presenting the *CyberTUM* prosthesis, developed by students as part of practical coursework since 2019. During several semesters of the course, multiple revisions mainly focused on improving the structure and mechanism were made to the prosthesis. The resulting third mechanical design iteration, with minor revisions to the electronics, was used for the competition. Although the design was promising, only a 12<sup>th</sup> place finish was achieved by the team. Based on the experience, more emphasis was placed on the mechanical iterations than on the electronics, which in their current state, would not support the additional features and functionality required to improve the prosthesis. This motivated the development of a new electronics platform with additional capabilities necessary for future generations of the prosthesis.

## 1.2. Research Aims

The aim of this work was to develop an embedded electronic platform to enable the research and development of an improved trans-radial prosthesis by students of the *CYBATHLON* project course offered at TUM. The focus of the course is the development of an improved prosthesis in the lead-up to the *CYBATHLON 2024* Competition. The platform developed needs to be capable of acquiring the required signals and driving the actuators of the current prosthesis design, while also including additional capabilities to facilitate improvements. Finally, the platform needs to be robust, flexible and expandable to support new variants of the prosthesis without the need to completely re-design the electronics for each iteration. To achieve this goal it was necessary to:

- Leverage the lessons learned during the *CYBATHLON 2020* Competition.
- Evaluate the electronics platform of the current *CyberTUM* prosthesis and identify limitations and potential improvements needed.
- Analyse the current state-of-the-art powered hand and arm prosthetic systems, from an electronics and embedded systems point of view, and select important features to incorporate into the new electronics platform.
- Develop a functional prototype which provides the required hardware, firmware and documentation to enable future students of the *CYBATHLON* course to continue development of the next generation of *CyberTUM* prosthesis.

## 1.3. Thesis Scope

The development scope for a trans-radial prosthesis is vast; as such, it was necessary to limit the scope of the electronics platform to a manageable level. There were also several factors which impacted the design of the electronics platform that needed to be considered. The solution proposed represents a compromise between complexity and functionality. The scope of development also needed to be restricted to achieve the research aims outlined in the previous section, within the time constraints imposed.

- Mechanism selection and mechanical design of a prosthesis affects many factors including the number of actuators required, which in turn influences the electronics required. This determination is considered outside of the scope of this work. The decision on the actuators supported by the platform was based on the state-of-the-art analysis and review of the current platform in order to cater for anticipated future improvements and requirements.
- Development effort was focused on lower level hardware design and firmware level software implementation to facilitate tasks such as motor control and sensor feedback.
- Higher level tasks such as overall prosthesis control and coordination, sensor signal feature extraction and interpretation were not considered.

## 1.4. Outcomes

A functional prototype of the improved electronics platform was successfully designed, fabricated and tested. A summary of the notable outcomes and improvements include:

- A 290% decrease in electronics footprint, while providing additional features and functionality.
- Cascaded control of four independent [BLDC](#) motors, double that of the current platform.
- Flexible and expandable design which allows functions on dedicated expansion slots to be altered without affecting the rest of the platform.
- Improved [EMG](#), analogue sensor implementation and support for digital sensors.

## 1.5. Structure of this Work

**Chapter 2** familiarises the reader with basic mechanics and nomenclature of the human arm, followed by a taxonomy of all human grasp patterns and the compromises necessary due to current technological limitations. The most important grasp patterns needed to maximise functionality in [Activities of daily living \(ADL\)](#), while limiting the complexity to a level manageable with current technologies, will be presented. A summary of the common [Human Machine Interface \(HMI\)](#) methods based on human bio-potential level signals found in literature, with special emphasis on determining the notable electrical characteristics of these signals, is provided. An analysis of the *CyberTUM* prosthesis highlights the limitations and potential improvements, while a state-of-the-art analysis of current commercial and research prostheses identifies common trends and provides the basis for the selection of desirable features incorporated into the platform design.

**Chapter 3** presents the results of the preliminary analysis performed with evaluation hardware provided by [MIRMI](#). The focus was on validating the cascaded motor control implementation and determining the computation requirements of the selected control and communication implementation before any new hardware was developed. These results were important to confirm the suitability of the microcontroller required to realise the electronics platform.

**Chapter 4** delves into the detailed design of the electronics platform. The identified design requirements are summarised and are based on the analysis performed in the preceding chapters. The overall scope of the platform is defined and leads into the component selection and design justifications phase. The definitive design architecture based on the selected components is then presented and the important design details of the various hardware elements developed are discussed. In addition to the hardware developed, details regarding the firmware implementation and drivers necessary to operate the diverse hardware elements are provided.

**Chapter 5** presents the test bench created to enable firmware development and testing of the electronics platform. Various tests were performed to obtain the data plots used to evaluate the performance of the system developed, including the coordinated control of all the actuators and the sensor acquisition systems developed.

**Chapter 6** provides a summary of the results achieved and details of remaining future work.

## 2. Background

Historically, most prosthetic devices available to amputees have been purely aesthetic. Body powered prosthesis were amongst the first attempts to restore a limited subset of the functionality of a missing limb. Recent advances in technology have allowed for increasingly sophisticated, externally powered devices to restore more of the lost functionality, while enabling more intuitive control of the prosthesis. However, even current state-of-the-art prosthesis are expensive, lack functionality, are heavy, uncomfortable or difficult to use. Therefore, research in this area is highly encouraged.

To develop an upper limb prosthesis, we first need to study the human hand/arm system to gain an understanding of the anatomy, mechanics and abilities that a prosthesis must attempt to replicate. Intuitive control of increasingly sophisticated prosthetic devices is also key to ensuring widespread adoption and acceptance for users of a prosthesis. Myoelectric prostheses provide a [Human Machine Interface \(HMI\)](#) based on bio-signal interpretation and currently show the most promise to restoring lost functionality while also enabling intuitive control. The current state of [HMI](#) is examined to understand the trends and requirements to use these control methods.

In order to establish common trends and identify potential improvements and new features, the current *CyberTUM* prosthesis, existing commercial and research designs are studied. Based on this analysis, the relevant desirable features and functions can be selected to form the requirements for a new, more capable electronics platform for future students to develop the next generation of the *CyberTUM* prosthesis.

### 2.1. Anatomy & Analysis of the Human Arm

The arm is a highly evolved limb which enables a wide range of delicate sensory-motor tasks. The arm is made up of a complex musculoskeletal structure comprised of a hand, forearm and upper-arm. The hand, positioned at the end of the upper limb, is comprised of four fingers and a thumb with complex joints whose function is to manipulate and grasp objects. This is possible due to fine motor control capabilities, precise sensory feedback and an opposable thumb. The hand is connected to the forearm via a wrist which allows the whole hand to move along two axes. The forearm connecting the wrist to the elbow enables rotation of the whole hand. The Upper-Arm connects the hand and forearm to the elbow and shoulder which provides the remaining range of motion. This section aims to supply basic anatomical concepts and nomenclature needed to understand the forearm, wrist and hand structures relevant to the trans-radial prosthesis use-case.

### 2.1.1. Degrees of Freedom (DOF)

The motion capabilities of the hand/arm system are determined by its complex musculoskeletal structure, which can be classified into 29 individual degrees of freedom using a the model shown in Figure 2.1a and 2.1b. In the case of the trans-radial amputation, the DOF above the forearm and including the elbow remain intact. As such, the remaining 24 are distributed as follows: four in each finger, three for extension and flexion and one for abduction and adduction. The thumb is more complicated and has five DOF, leaving three DOF for the rotation and translation of the wrist [ES03].

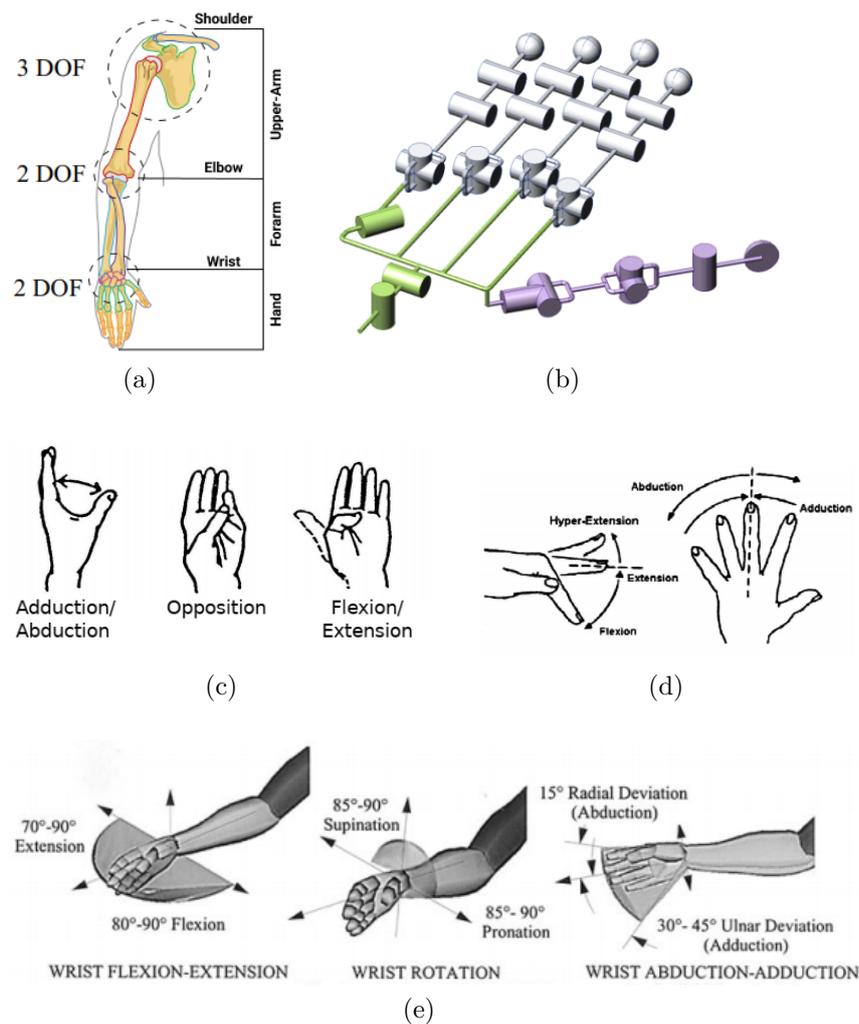


Figure 2.1.: (a) DOF of arm, excluding the hand [Gho18] (b) DOF of hand and wrist [Sha] (c) Movement Patterns of the Thumb, (d) Fingers & (e) Wrist [Kut09]

The following terminology is commonly used. For fingers, *flexion* and *extension* are the formal names for the closing and opening motions respectively. *Abduction* corresponds to laterally spreading the finger out, away from its resting position; *adduction*, is the opposite. In addition to these movements, the thumb is also capable of *opposition*, the movement generally involved in pinching. Finally, whole hand rotation(*pronation/supination*) is facilitated by the forearm.

### 2.1.2. Grip Patterns & Common Activities

While the model presented in 2.1.1 defines all possible movements at a joint level, not all contribute or are necessary in everyday use cases. Trade-offs need to be made due the limitations on size and weight and complexity for a practical prosthesis. It is therefore necessary to perform a grip pattern analysis to prioritise the inclusion of the **DOF** which are used most frequently.

Extensive studies have been carried out in an attempt identify and classify a comprehensive set of human grasp behaviours. The work carried out by [Fei+16] aims to compare all human grasp taxonomies provided in the literature to find the largest set of distinct grasps, and synthesises them into a single classification. The 33 distinct grasps identified are summarised in Figure 2.2.

		Power					Intermediate			Precision				
Opp:	Palm	Pad				Side			Pad				Side	
VF:	3-5	2-5	2	2-3	2-4	2-5	2	3	3-4	2	2-3	2-4	2-5	3
Thumb Abducted	1: Large Diameter	31: Ring	28: Sphere 3 Finger	18: Extension Type	19: Distal Type	23: Adduction Grip		21: Tripod Variation	9: Palmar Pinch	8: Prismatic 2 Finger	7: Prismatic 3 Finger	6: Prismatic 4 Finger	20: Writing Tripod	
	2: Small Diameter			26: Sphere 4-Finger					24: Tip Pinch	14: Tripod	27: Quadpod	12: Precision Disk		
	3: Medium Wrap								33: Inferior Pincer			13: Precision Sphere		
	10: Power Disk													
	11: Power Sphere													
Thumb Adducted	17: Index Finger Extension	4: Adducted Thumb				16: Lateral	25: Lateral Tripod						22: Parallel Extension	
	5: Light Tool					29: Stick								
	15: Fixed Hook					32: Ventral								
	30: Palmar													

Figure 2.2.: Taxonomy of Human Grasp [Fei+16]

Based on the number of grasping patterns identified above, it is clear that The primary function of the powered prosthetic arm should be to restore as many of the the grasping patterns used in day-to-day activities as possible [Fei+16]. These activities are commonly referred to as **Activites of daily living (ADL)**.

Recent developments in myoelectric prostheses have focused on increasing dexterity, speed and improving control strategies. However, these improvements often come at the cost of increased weight, size, and complexity, which reduces robustness and affordability as the necessary actuators, transmissions, and electronics must be housed within the device. Given these design constraints and the limitations of current control strategies, replicating the full kinematics and grasp patterns possible with the the human arm is not feasible.

For this reason, methods such as the [Southampton Hand Assessment \(SHAP\)](#) [Mer03] have been developed to assess functionality of prosthetic devices and is based on a reduced subset of the most commonly used grasps that are considered particularly useful for completing common ADL. The reduced set of grasps is shown in [Figure 2.3](#)

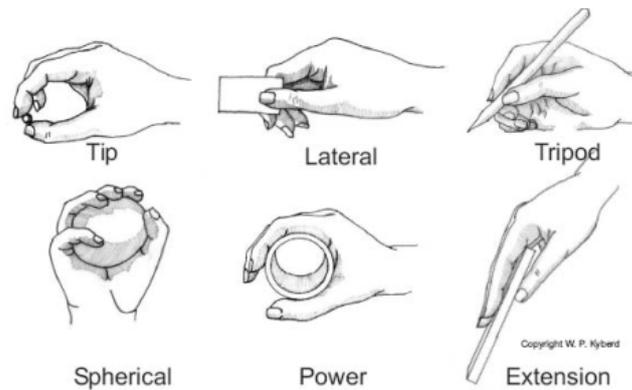


Figure 2.3.: Grip types used in Activities of Daily Living [Mer03]

According to [Sem+16], the *Power* grasp or variation there of, is the mostly employed pattern with a frequency of 35% of ADL, followed by *precision/tripod* and *lateral* grasp at 30% and 20% respectively. The remaining 15% is made up of some variation of the grasp types identified in [Figure 2.2](#) and are used less frequently. From these statistics, it is clear that for a prosthesis to be considered successful, it must prioritise these commonly used grasp patterns and execute them robustly.

### 2.1.3. Degrees of Freedom (DOF) & Degree of Actuation (DOA)

A recent study by [MCC15] reveals that historically, research has focused heavily on the development of ever more sophisticated artificial hands, capable of multiple grasps; but, less research focus has been devoted to wrist design, despite the fact that the wrist contributes significantly to the execution of upper limb motor tasks. The study showed that a 22-DOF hand with a 1-DOF wrist is functionally equivalent to a 1-DOF hand and a 2-DOF wrist when performing the activities of daily living assessed by the SHAP.

The embedded platform proposed by this thesis must offer flexibility and provide support for future mechanical designs which explore different configurations in DOF and DOA. Based on the findings presented by [MCC15], a design supporting 4-DOF is considered sufficient and forms part of the design criteria. The final configuration of these DOF will be based on the analysis of the limitations of the current platform and comparison with other state-of-the-art devices in subsequent sections.

## 2.2. Human-Machine Interfaces for Upper Limb Prosthesis Control

As previously established, the human forearm is an incredibly sophisticated mechanism and replacing the natural bidirectional communication between the nervous system and the human arm presents a significant challenge. The **Human Machine Interface (HMI)** is the primary control method for the user of the prosthesis and is a vital part of the user experience. A large variety of **HMI** solutions have been developed and evaluated in literature. The most advanced and promising of these solutions rely on bio-signals to interpret user intent to control the prosthesis.

### 2.2.1. Common HMI Methods

A recent survey by [AKM21] evaluates the current state-of-the-art in **HMI** techniques for upper limb prosthetic devices and provides an overview of acquisition, pre-processing and processing techniques, which form the basis for all **HMI** solutions. The survey is based on a curated list of 45 papers with a focus on bio-signals and signal processing methods for upper-limb prosthesis control. The results are shown in Figure 2.4. From this data it is evident that the most research effort is currently directed towards solutions which incorporate **Electromyography (EMG)**, accounting for approximately 80 percent of the surveyed papers.

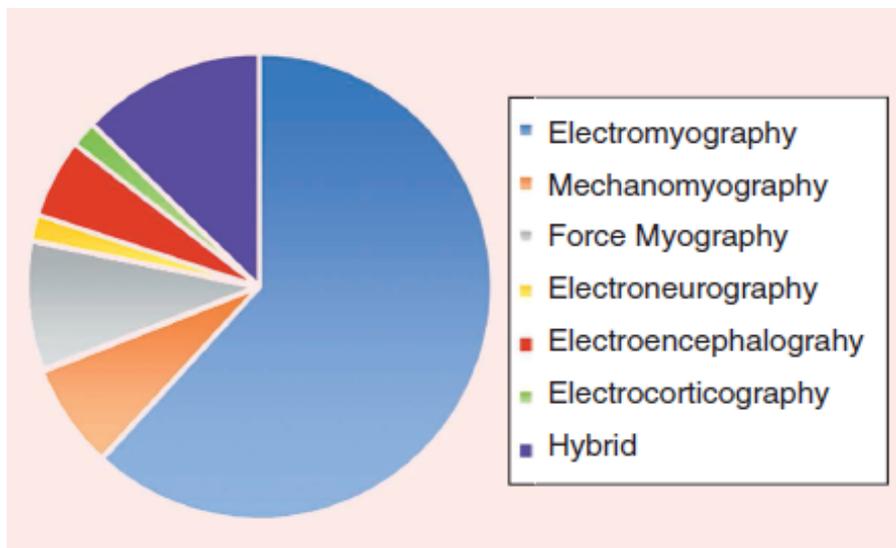


Figure 2.4.: Prevalence of different Bio-signals used in **HMI** Applications [AKM21]

In recent years, **Surface Electromyography (sEMG)** has become one of the primary control method of prosthetic hands due to the comfort and naturalness offered [TBL17] and designs have developed to meet the demands of upper limb amputees. Devices have evolved from early on-off, proportional and state machine control to more advanced techniques, such as pattern recognition based control [Asi+20]. Due to this widespread adoption, and clear potential as a primary control mechanism, **EMG** was selected as the primary control method for proposed electronics platform, in favour of the other **HMI** approaches.

### 2.2.2. Types of EMG

EMG is a technique used to record electrical signals from the muscles during neuromuscular activity [Asi+20] and can be categorised into two main groups: internal EMG which requires an invasive procedure to implant electrodes inside target muscle groups and sEMG with electrodes on the skin. Despite the inherent crosstalk experienced during deep and superficial muscle activation, sEMG is still preferred due to its non-invasive nature, even with the signal detection and quantification difficulties [AKM21].

The use of internal EMG is excluded as the TUM CYBATHLON team relies on a volunteer amputee pilot. The invasive procedures required to utilise internal bio signal electrodes are not feasible and makes testing and development using able bodied subjects impossible.

### 2.2.3. EMG Signal Properties

The field of bio-signal acquisition and their interpretation using post processing and pattern recognition techniques is vast, so it was necessary to limit the scope. The focus was limited to examining the characteristics of the sEMG signals, in order to understand the acquisition hardware requirements. Techniques for feature extraction and the practical classification pipeline are not considered.

The amplitude of an EMG signal is of a stochastic nature and can be represented by a Gaussian distribution. The EMG signal amplitude ranges from 0 to 10mV (*Peak-to-peak*) or 0 to 1.5mV (*RMS*) with dominant energy in the 0-500Hz band. The main information of interest resides in the 50 to 150Hz range [Car02]. The amplitude and frequency of commonly used bio-potential signals and the frequency distribution is shown in Figure 2.5.

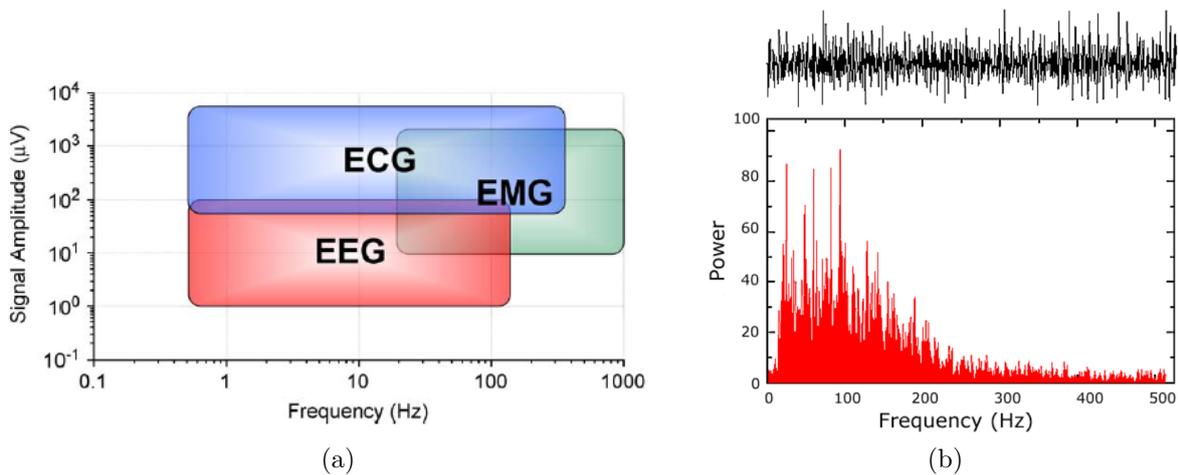


Figure 2.5.: (a) Frequency and amplitude characteristics of commonly used bio-potential signals [Yaz+09] (b) Frequency Spectrum of a typical EMG signal [Car02]

The stochastic nature and low amplitude of the **sEMG** means that readings are susceptible to various sources of noise and are extremely sensitive to electrode placement and proper skin preparation. The signal is also susceptible to noise sources such as power line harmonics (50 or 60 *Hz*). For this reason, specialised hardware is required to filter, amplify and digitise the **sEMG** signal for later use in a robust interpretation and classification **HMI** system. An example of the signal such a system interpret is shown in **Figure 2.6**

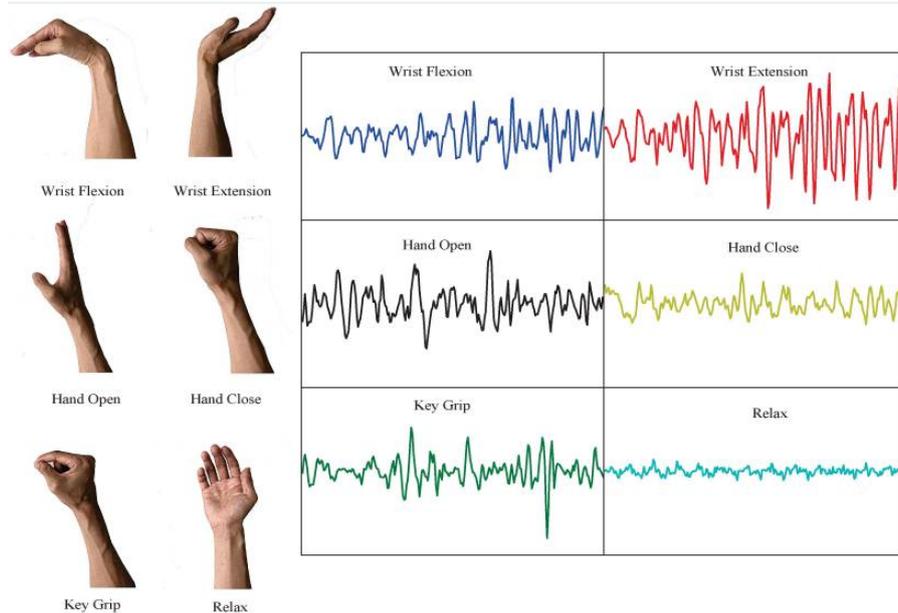


Figure 2.6.: EMG Application Example [She+19]

## 2.3. Existing TUM Cybathlon Prosthesis

The **TUM CYBATHLON** student team was founded in the Summer Semester (SoSe) 2019 with the goal of developing a powered arm prosthesis to compete in the **CYBATHLON 2020** Competition. The design of the prosthesis was refined each semester during a practical project course offered at the **MIRMI**. The author was involved with development of the electronics and embedded software in the Summer Semester (SoSe) 2020. The chronological progression of the design from the early prototypes to the final Competition device is shown in **Figure 2.7**.

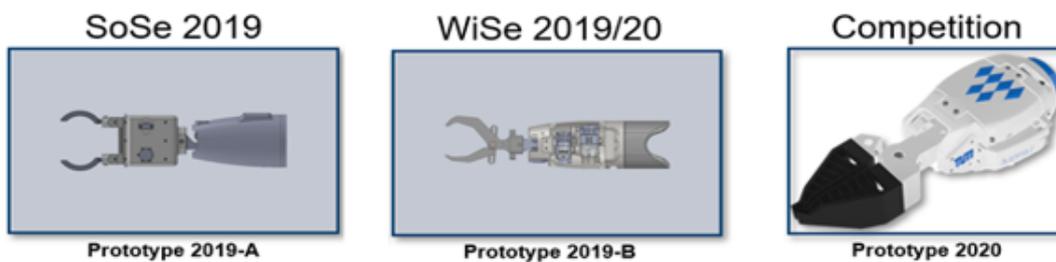


Figure 2.7.: Design Iterations TUM Prosthesis

### 2.3.1. Electronics Platform Architecture

The overall architecture of the *CyberTUM* prosthesis is shown in Figure 2.8

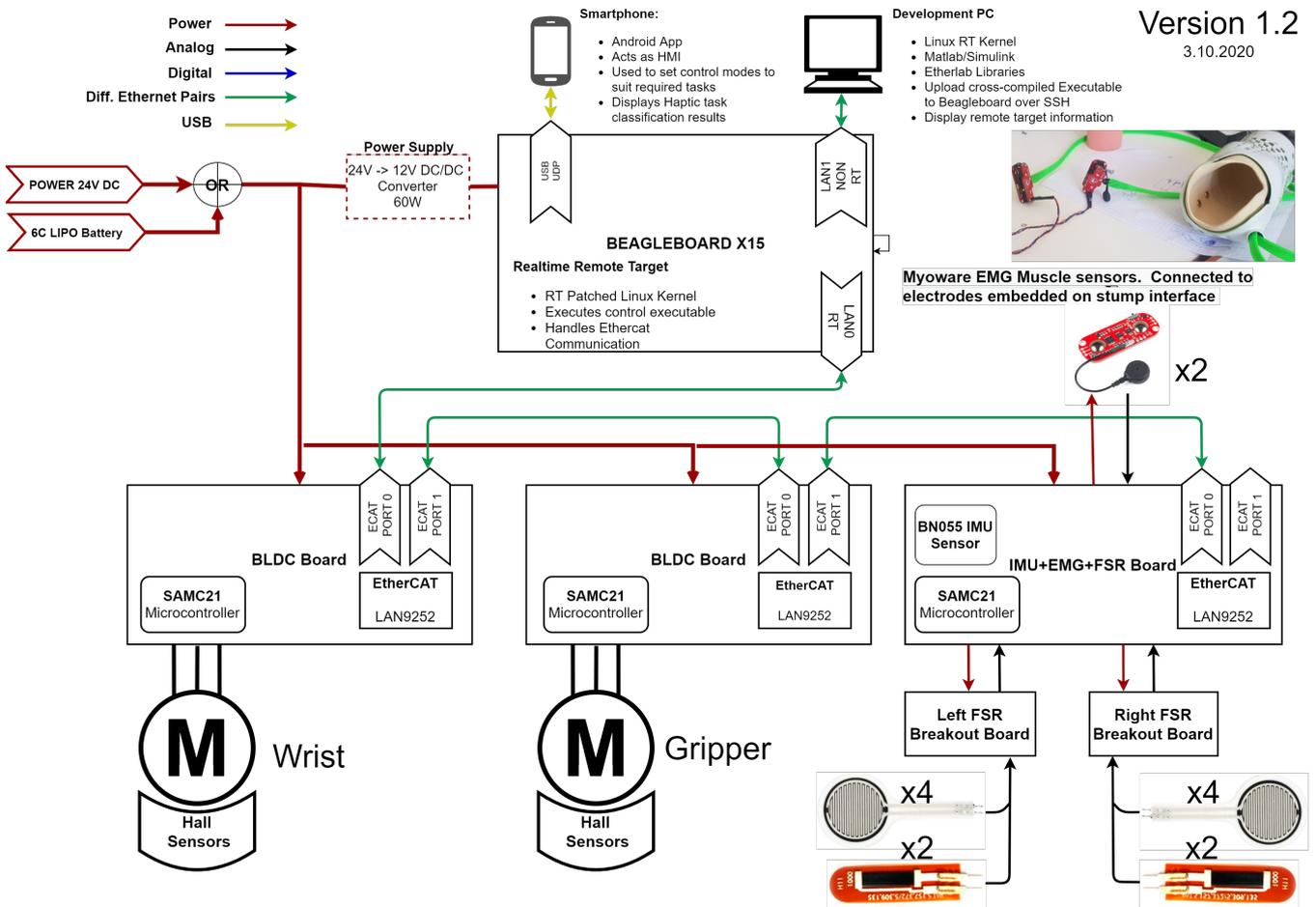


Figure 2.8.: *CyberTUM* prosthesis Block Diagram

Separate control boards were used for each of the BLDC actuators. The control of these motors was limited to position control, with *Six-step Commutation (6SC)*. No link side position feedback was possible, hence the gripper and wrist required calibration at power up and all motions were relative to this initial calibration. The sensor board included an *Inertial measurement unit (IMU)* and support for analogue sensors only. Twelve channels were dedicated to the *Force-Sensing Resistor (FSR)* sensor array used for tactile sensing. Wiring to the gripper was simplified with two signal distribution boards. Two additional analogue channels were connected to off the shelf *MyoWare* Muscle Sensor kits.

These three discrete controllers were linked via a real-time capable *EtherCAT* communication bus to a *Beagleboard Single Board Computer (SBC)* which implemented the high level control algorithms developed in *Simulink* and provided *EtherCAT Master* functionality.

### 2.3.2. System Design

While the overall design of the system was refined each semester, the general configuration and design language remained the same. The system retained the two actuator, tendon based drive system with a 1-DOF scissor style gripper design. The 2-DOF wrist also retained powered *flexion/extension* and manual wrist *rotation*. Design iterations were usually conservative as there was a limited budget available for the student project and fabrication was largely limited to 3D printed designs. The host institute provided the actuating units and majority of the electronics which were re-purposed from other projects at the institute. A high level overview of the mechatronic system is shown in [Figure 2.9](#).

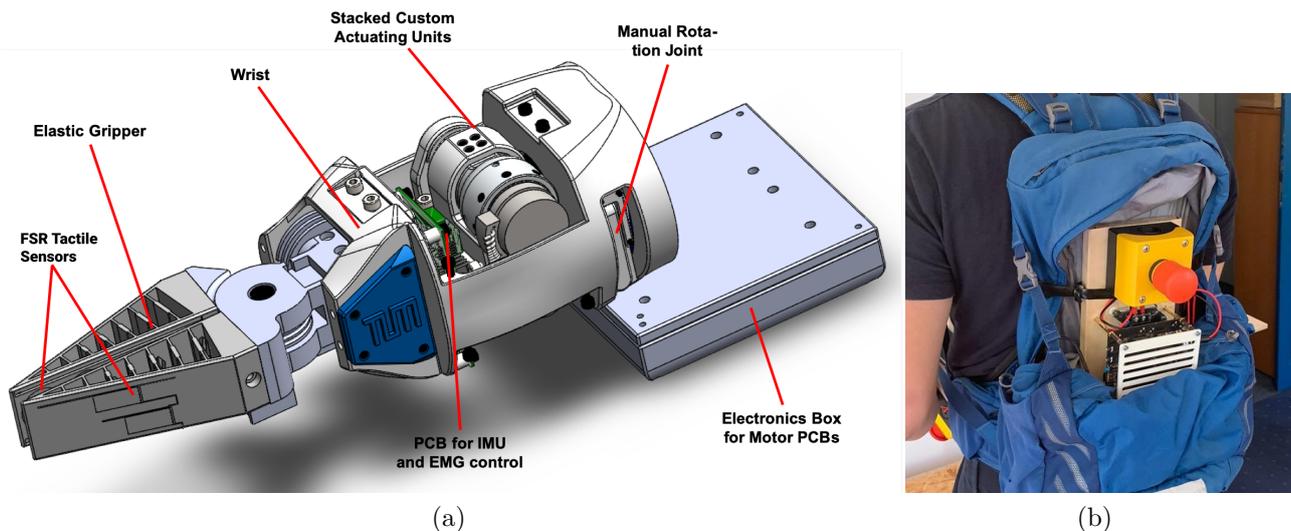


Figure 2.9.: (a) *CyberTUM* Prosthesis (b) Backpack containing high level controller and Battery

The majority of the electronics development effort was focused on overall integration of all electronic components, as well as implementing and improving the sensor acquisition system needed for the [HMI](#). The High level controller was responsible for the overall control of the prosthesis based on the users inputs. A finite state machine containing the appropriate states for each of the competition tasks was used. The system also implemented a pattern recognition system that was trained to classify the [EMG](#) and [FSR](#) data to determine user intent and recognise objects for the haptic task in the competition.

The [TUM](#) student team was fortunate to have the same volunteer pilot meeting the competition requirements since the the team was founded. This consistency was vital as the design was strongly influenced by the pilots physical proportions and feedback regarding comfort and task completion methodology.

### 2.3.3. Specifications

The key specifications for the *CyberTUM* prosthesis are summarised in [Table 2.1](#)

TUM Cybathlon Prosthesis	
<b>Motors</b>	2(BLDC)
<b>Motor Control</b>	Six-step Commutation (6SC) with Position control
<b>Transmission</b>	Harmonic Drives & tendons
<b>DOF</b>	3 <sup>1</sup>
<b>Mechanism</b>	Tendon Based with compliant gripper
<b>HMI Interface</b>	EMG <sup>2</sup> , Smartphone App, FSR <sup>3</sup>
<b>Feedback</b>	Relative Motor Position, FSR based grip force measurement, Pattern recognition based tactile sensing for object recognition
<b>Controllers</b>	3 Discrete control boards
<b>Microcontrollers</b>	Microchip SAMC21 series
<b>Sensors</b>	FSR (12 Ch), IMU, EMG (2 Ch)
<b>Operating Voltage</b>	24V
<b>Communication</b>	EtherCAT (1kHz)
<b>Control Strategy</b>	Distributed with Hardware Abstraction Layer (HAL)
<b>Max Grip strength</b>	Not Measured

<sup>1</sup> 1 in gripper, 2 in the wrist, manual wrist rotation

<sup>2</sup> EMG pattern recognition abandoned for competition

<sup>3</sup> Proportional FSR based Head sensor was used for gripper control in conjunction with Smartphone for grip selection

Table 2.1.: *CyberTUM* prosthesis key specifications

### 2.3.4. Limitations & Potential Improvements

The *CyberTUM* prosthesis was able to compete in the 2020 competition and despite the limited development time and promising initial results, only a 12<sup>th</sup> place finish was achieved as several key race tasks could not be successfully completed. Some examples include the haptic box challenge, where not all objects were successfully classified, others had to be skipped as the prosthesis or gripper were physically too large. These lessons learned serve as motivation for further improvements, to ensure more tasks can be completed in the future. Potential improvements, with a particular focus on the electronics platform, are listed in [Table 2.2](#).

Aspect	Description
<b>DOF &amp; DOA</b>	The 3-DOF, 2-DOA configuration and scissor style compliant gripper design limited the grasps achievable. Support for additional actuators to power additional DOFs in the gripper and an active wrist would significantly improve grip performance and usability as the manual wrist adjustment mechanism was cumbersome.
<b>Motor Control Strategy</b>	The motor control strategy for the competition prosthesis only supported position control. Cascaded Position, Velocity and Current control would improve grasping performance and allow for improved control of grip forces.
<b>Position Feedback</b>	The position feedback system was limited to the incremental feedback signal provided by the hall sensors integrated in the motors. All positional reference is lost at power-up and the prosthesis needs to be calibrated to perform relative movements. An absolute position sensing system on the link side is seen as essential to control the prosthesis while also eliminating the need to calibrate the prosthesis.
<b>Tendon Tension</b>	The tendon based design also experienced issues maintaining tension in the tendons. Position feedback was only available on the motor side, and not at the link side. Inconsistent tension impacted the position controller performance significantly as slack in the tendon or slip on the pulley could not be detected or compensated for. Link side sensing is seen as the key to reliable performance of the tendon design.
<b>Tendon Friction</b>	Friction in the tendon based mechanism and compliant gripper design required large motors to overcome both the friction and to deform the compliant gripper enough to securely to grasp different object shapes.
<b>General Dimensions</b>	The size and weight of the prosthesis meant several competition tasks such as wearing and zipping up of a jacket could not be completed as the prosthesis was physically too large to fit through a jacket sleeve. The overall weight also made prolonged use uncomfortable. The size of the prosthesis was largely dictated by the size of the required actuation units and control electronics. Improvements in the mechanism design and electronics could potentially allow for smaller motors and control boards, which are more easily accommodated.

<b>Backpack Storage</b>	In addition to the motors and control electronics, the need for a battery and the high level control PC, meant that a backpack was required to accommodate all the components. An improved electronics design, suitable battery and more compact embedded PC could eliminate the backpack which would improve the user experience.
<b>EMG</b>	The <i>MyoWare</i> series of Muscle sensors used offered inconsistent performance and the signal to noise ratio of the data obtained was poor. The form factor also proved to be difficult to integrate into the prosthesis.
<b>FSR Integration</b>	Twelve FSR type sensors were integrated into the compliant gripper design. These sensors provided the necessary input signals to the machine learning based recognition system used to classify objects during the haptic task of the competition. Integration in the compliant gripper was difficult and the fragile sensors were easily damaged. The classifier was trained with a full complement of sensors, but extended use lead to sensor failures which affected the classification accuracy of the system.
<b>FSR Signal Conditioning</b>	The simple voltage divider configuration used for signal conditioning was not optimal due to the exponential resistance characteristics of the sensors used. The sensors quickly saturated to their full scale reading, which affected the achievable force detection resolution. This saturation behaviour and limited force resolution likely impacted classifier performance. A solution which exploits the linear conductance properties of FSR sensors would improve the quality of the tactile feedback signals.

Table 2.2.: Limitations and Potential Improvements

## 2.4. State-of-the-Art in Powered Upper Limb Prostheses

A Considerable number of anthropomorphic, under-actuated designs exist in literature that mimic finger and wrist movements based on linkages and tendon mechanisms. The majority of commercial, recent research devices follow a similar design pattern as shown [Figure 2.10](#). The following section will briefly analyse the state-of-the-art in upper-limb prosthesis and dexterous robotic arm systems.

Examples of both commercially available and research prosthesis devices, as well as dexterous arm systems are analysed. The examples were selected to deliberately include both prosthetic devices indented to compensate for missing limbs and anthropomorphic dexterous robotic arm systems used in humanoid robotics research. While the end use-cases and constraints are different, the innovations and ideas developed complement each other and are important to consider for future developments.

Relevant comparisons to the existing *CyberTUM* prosthesis are made and pertinent technologies required to realise a future prosthetic device which is both competitive for the specific *CYBATHLON* race tasks as well as general [ADLs](#) are identified.

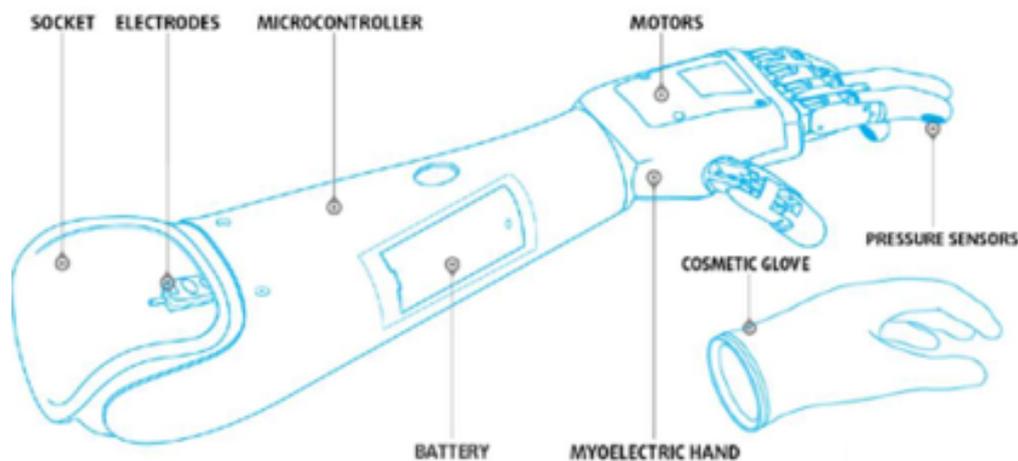


Figure 2.10.: Common Prosthesis configuration [[CSM19](#)]

### 2.4.1. Commercially Available Products

Detailed information about commercially available prosthetic devices, especially information related to the hardware, electronics and control algorithms is difficult to obtain due to intellectual property and commercial restrictions. As such, the commercially available products are analysed at a higher level and provide an indication of which approaches are commercially viable and most successful with end-users. An important distinction between prototype research hands and commercial devices is that prototypes are often developed to demonstrate a particular feature or concept, not to prove an entire system, and therefore do not need to meet the same requirements of commercial hands. The commercial devices reviewed are shown in [Figure 2.11](#) and the specifications are summarised in [Table 2.3](#)

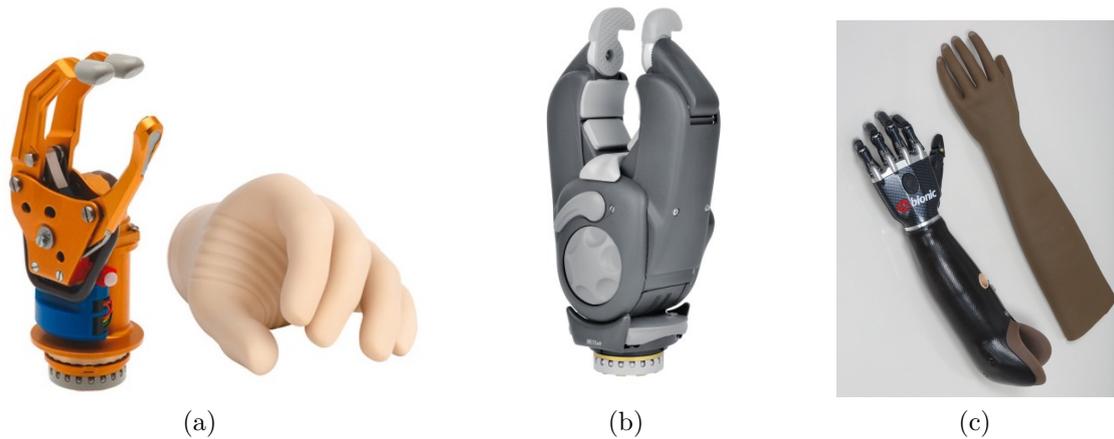


Figure 2.11.: (a) Sensor Hand Speed (SHS), (b) System Electric Greifer (SEG) and (c) Be-bionic Hand (BBH)

### SensorHand Speed & System Electric Greifer

The first commercially available prosthesis to be reviewed is the the single **DOF** Otto Bock **Sensor Hand Speed (SHS)** shown in [Figure 2.11](#). According to [[Kut09](#)], despite more advanced solutions being available on the market, the **SHS** is still the defacto standard for externally powered hand-like prosthetic devices. It is still the most commonly prescribed prosthetic solution because, for many users, it strikes the right balance in robustness, speed, grip strength and ease of use. In addition, this option is significantly cheaper and therefore more widely accessible when compared to newer, more complicated devices.

The device essentially consists an internal tri-digit structure that closes in a C-shape for power or pinch grasp with force and velocity control to adjust grip strength. The **SHS** is available with an optional cosmetic glove shown to aid aesthetics, with a trade-off in mechanism performance [[Kut09](#)]. The fully integrated electronics and an industry standard quick disconnect system provide a wrist rotation option. The **System Electric Greifer (SEG)** is functionally similar to the **SHS** but opts for a non-anthropomorphic, power assisted design. Both devices allow simple, voluntary control in both open and close directions and perform a single, rigid grasp.

These two systems are functionally the most similar to the *CyberTUM* prosthesis due to their limited number of **DOF** and **DOA**. However, they prove that the anthropomorphic, multi-finger approach is not necessarily superior in functionality and user acceptance.

### Be-bionic 3

Compared to the relatively simple **SHS**, the **Be-bionic Hand (BBH)** produced by OttoBock is significantly more complex. The design features six active **DOF** and each finger has bespoke linear actuators and a *synchronous* mechanism. The *synchronous* mechanism limits the amount of actuators required without losing functionality by coupling joints with a linkage mechanism, whose movement can be described by a single parameter and can be counted as a single **DOF**. A combination of five of these mechanisms, driven by separate motors, allows the **BBH** to control

each finger individually in a motion similar to the human fingers. The mechanism also includes elements to allow a certain level of compliance to allow movement when an external force is applied to prevent damage and increase robustness.

The position of the thumb can be manually adjusted, providing *palmer* and *lateral* prehension. The hand is capable of 14 preset grip patterns including *power*, *intermediate* and *precision* grasps, while also allowing the users to create their own customised grips. The hand is combined with the socket interface pictured in Figure 2.11 and is available with an additional active wrist actuator to rotate the whole hand, but does not support any additional wrist DOF.

The BBH user interface is provided by buttons on the back of the hand which cycles through available grips. Proportional control of selected grasps is realised by interpreting signals from muscles in the residual limb, with one or two Electromyography (EMG) electrodes. The latest models include additional "Myo Plus" hardware and software which claims to use advanced pattern recognition techniques to learn to interpret the user's intentions based on EMG data to execute specific movements. A smartphone app is provided to allow for calibration and customisation to the individual user via Bluetooth.

### Specification Summary

	SHS	SEG	BBH
<b>Motors</b>	2(DC)	2(DC)	5(DC) <sup>1</sup>
<b>Transmission</b>	N/A	N/A	Bespoke linear actuators
<b>DOF</b>	2 <sup>2</sup>	2 <sup>2</sup>	6 <sup>1</sup>
<b>Mechanism</b>	Tri-digit C-shape	C-shape	Synchronous
<b>User Interface</b>	EMG <sup>3</sup>	EMG <sup>3</sup>	Button, EMG <sup>4</sup>
<b>Feedback</b>	Thumb & Grip Force Sensor, EMG	Grip Force Sensor, EMG	Fingertip force Sensors, EMG
<b>Sensors</b>	Position & speed sensor	Position & speed sensor	Position, current
<b>Max Grip strength</b>	High (100N)	High (160N)	Power (75N), Precision (35N)
<b>Communication</b>	N/A	N/A	Bluetooth
<b>Control Strategy</b>	Centralised	Centralised	Centralised

<sup>1</sup> 5 in hand, 1 with optional wrist rotator

<sup>2</sup> 1-DOF Gripper, 1-DOF Wrist

<sup>3</sup> Proportional control of grip force and closing speed

<sup>4</sup> Proportional control or pattern recognition with latest generation

Table 2.3.: Sensor Hand Speed (SHS), System Electric Greifer (SEG) & Be-bionic Hand (BBH) key specifications

### 2.4.2. Research Prostheses & CYBATHLON Competitors

The goals of a research prosthesis and a commercial prosthesis are often very different. The research devices selected in this section demonstrate different concepts and approach the underlying problem differently, despite all being anthropomorphic, dexterous hand designs. The differences in research focus result in vastly different designs, but the basic components and requirements remain the same.

The first research device to be reviewed is the [SoftHand 2 Pro \(SH2-P\)](#), which takes the concept of adaptive under actuation to the extreme by achieving high dexterity with only 2 actuators. [sEMG](#) is used to interpret user intentions based on muscle signals from sensors on the residual limb to execute a different grasps. The next device is the [Deutsches Zentrum für Luft und Raumfahrt Hand Arm System \(DLRHAS\)](#), which is not a prosthetic device and not intended as a limb replacement. This hyper-actuated humanoid robotic platform with 52 actuators demonstrates incredible dexterity and hardware sophistication in a form factor close to its human archetype in terms of size, weight and grasping performance.

These examples provide insights into the future of prosthetic arm design and the technologies explored may well find their way into the next generation of commercial products. The platform developed for this thesis aims incorporate elements from these research platforms that are considered important to provide a solid foundation for further research using the platform.

#### SoftHand 2 Pro

The *SoftHand* series of prostheses from Pisa/IIT has participated in the *CYBATHLON* since 2016 and proved to be very successful, taking first place among the myoelectric competitors each time. The system consists of a self contained anthropomorphic hand with manual wrist rotation. The main objective of this hand is to maximise mechanical robustness, compliance and dexterity with a minimum number of actuators. The first version of the [SH-P](#) with a single actuator and 2 Channel [EMG](#) system is shown in [Figure 2.12](#).

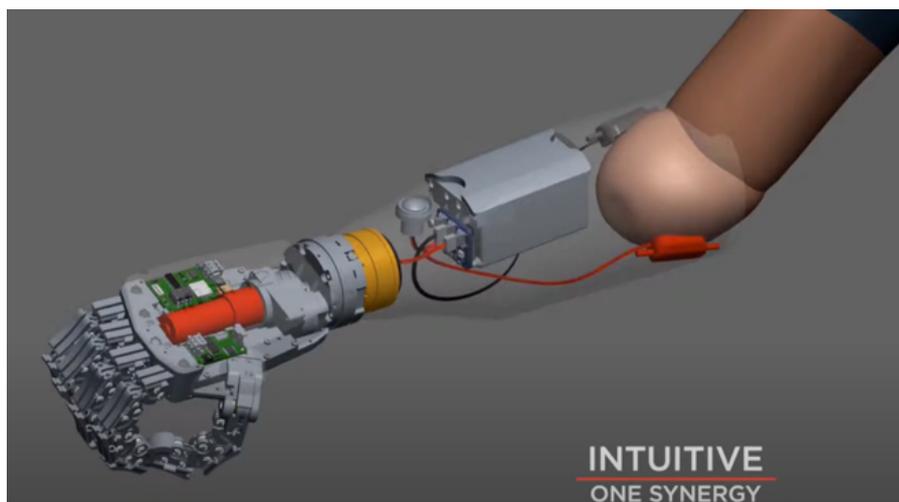


Figure 2.12.: Soft Hand Pro System [Pia+17]

The **SH2-P** employs an *adaptive under-actuation* system where a single actuator controls a number of independent **DOF**, often through the use of a cable or tendon. In contrast to *synchronous under-actuation*, a single actuator parameter cannot be used to describe the position of individual joints because they depend on contact state with the object being grasped. This allows fingers to passively adapt to the shape of the object being grasped and better distribute the contact force around the object, which can improve grip performance. [Figure 2.13](#) illustrates the differences.

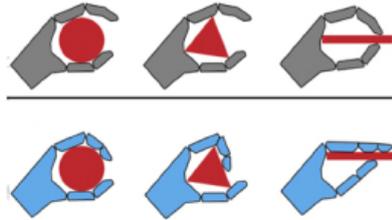


Figure 2.13.: synchronous vs Adaptive grasp [[Ope](#)]

The latest **SH2-P** shown in [Figure 2.14](#) adds a second actuator to improve fine grasp capabilities, strength and robustness while retaining the single tendon actuation design and the 19 **DOF** of its predecessor. To execute a variety of grasps as shown in [Figure 2.14](#), a novel control algorithm is used which uses the friction inherent in the tendon based mechanism as a design tool [[Pia+20](#)]. This approach proved to be very effective, allowing the device to complete a wide range of **ADL** and complete all the *CYBATHLON* competition tasks in record time.



Figure 2.14.: SH2-P System Overview [[Pia+20](#)]

The latest version also investigates a machine learning based classifier to distinguish user intentions based on muscle signals from up to eight **EMG** sensors, as opposed to the usual one or two. This allows the **SH2-P** to take advantage of the additional control inputs and the **DOF** to execute a wide range of grasps and hand manipulations. Additionally, according to [[Pia+20](#)], the addition of an eight channel **EMG** system and associated classifier helped improve control input performance, robustness and time performance of the test subjects during functionality testing when compared to the original two channel system.

SH2-P	
<b>Motors</b>	2(DC)
<b>Transmission</b>	Planetary Geartrain & tendons
<b>DOF</b>	20 <sup>1</sup>
<b>Mechanism</b>	Tendon Based adaptive under-actuation
<b>User Interface</b>	EMG <sup>2</sup>
<b>Feedback</b>	Tendon position and force
<b>Sensors</b>	Position, current sensors
<b>Max Grip strength</b>	Power (76N), Pinch (20N)
<b>Communication</b>	Serial (RS-485)
<b>Control Strategy</b>	Centralised

<sup>1</sup> 19 in hand, + 1 with manual wrist rotation

<sup>2</sup> Proportional control with 2 sensors, Pattern Recognition with 8 Sensors

Table 2.4.: SoftHand 2 Pro (SH2-P) key specifications

### Deutsches Zentrum für Luft und Raumfahrt Hand Arm System (DLRHAS)

The DLRHAS shown in Figure 2.15 is a sophisticated anthropomorphic research platform that focuses on robustness, dynamic performance and dexterity through novel intrinsic variable compliance joints. The DLRHAS introduces the concept of *hyper-actuation* and the complex mechanism draws inspiration from the structure of the biological hand and uses tendons, with two actuators per tendon, to realise the antagonistic drive compliance mechanism described by [Gre+12]. This design allows each actuated joint to be controlled independently and is the most dexterous design to date, but also the most complex. The design demonstrates impressive miniaturisation by embedding 38 control tendons, 430 sensors, 52 motors and various controllers all linked with high speed communication interfaces and hard real-time capabilities in a package that is close to its human archetype [Gre+11].

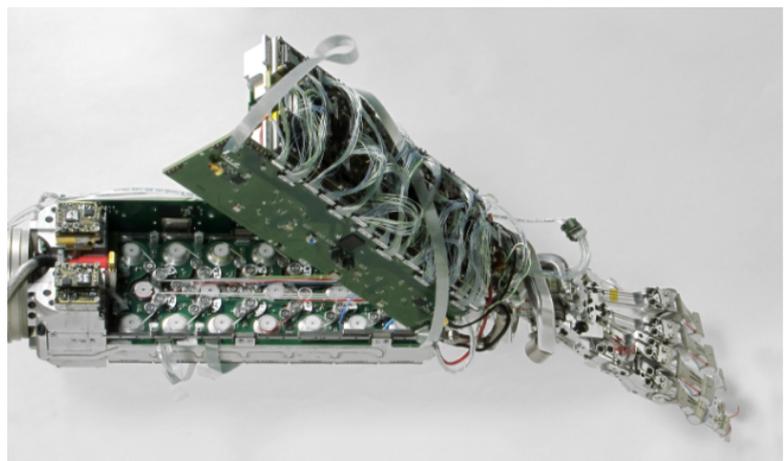


Figure 2.15.: Deutsches Zentrum für Luft und Raumfahrt Hand Arm System (DLRHAS) [Gre+11]

A survey by [Sem+19] reveals that the most common actuators used in prosthetic devices today are brushed **Direct Current (DC)** motors. They have historically been favoured over **Brushless DC (BLDC)** due to their ease of control. All the devices reviewed so far have used **DC** motors for actuation, while the **DLRHAS** opts for **BLDC** motors exclusively. **BLDC** motors have a higher power-to-weight ratio than comparable brushed **DC** motors, which in this design, is crucial as the weight and packaging size of the 52 motors needs to be minimised. More complex electronics and control strategies are required due to the electrical commutation and rotor angle sensing requirements. In this application, each motor has a dedicated angular position sensor, but this requirement can also be solved with lower resolution solutions, such as hall sensors often integrated into the motor. With recent advances in technology, the power-to-weight benefits of **BLDC** outweigh the historical drawbacks for prosthesis applications.

The *centralised* controller architecture employed by most myoelectric prostheses and designs reviewed thus far rely on a single embedded controller whereas the *distributed* controller architecture used by this complex mechatronic was able to achieve the goal of control loops beyond  $1kHz$  and provides several benefits. These include functionality encapsulation, re-usability and modularity, which are desirable for a research platform that is prone to change significantly during development. Individual components can be developed and tested independently and communication between components is achieved using standardised, real-time and deterministic interfaces, easing the integration into the complete system. Despite this, the seamless distribution of high-bandwidth control algorithms to heterogeneous platforms still proves to be a challenge [Jor+52].

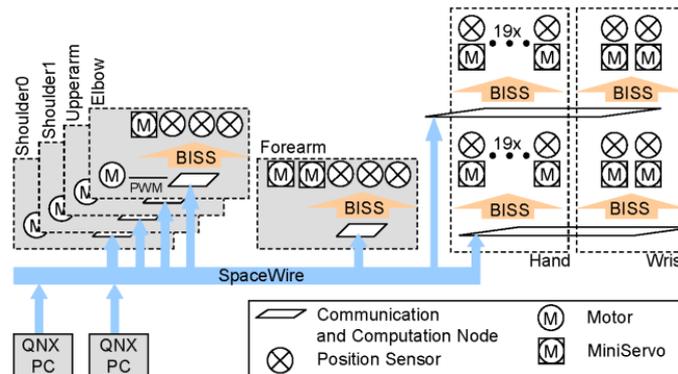


Figure 2.16.: DLRHAS distributed topology [Gre+11]

The **DLRHAS** makes extensive use of FPGA based computation, communication and low-level control modules to achieve the desired performance. Control is realised by a cascade control architecture with the inner control loop rates of  $100kHz$  for the low-level control modules. These modules are linked to several computation nodes via a synchronous *BiSS* interface. These nodes are responsible for signal aggregation and provide the *SpaceWire* communication backbone to the high-level host control loop. *SpaceWire* is a low footprint packet based bus that is deterministic for a given topology [Jor+52] and is comparable to other industrial *Ethernet* based field-buses such as *EtherCAT*. The outer host control loop targets  $3kHz$  loop rates and is realised on a PC based real-time capable host system (QNX). The topology described is shown in Figure 2.16. Implementation details for the hand system are summarised in Figure 2.17.

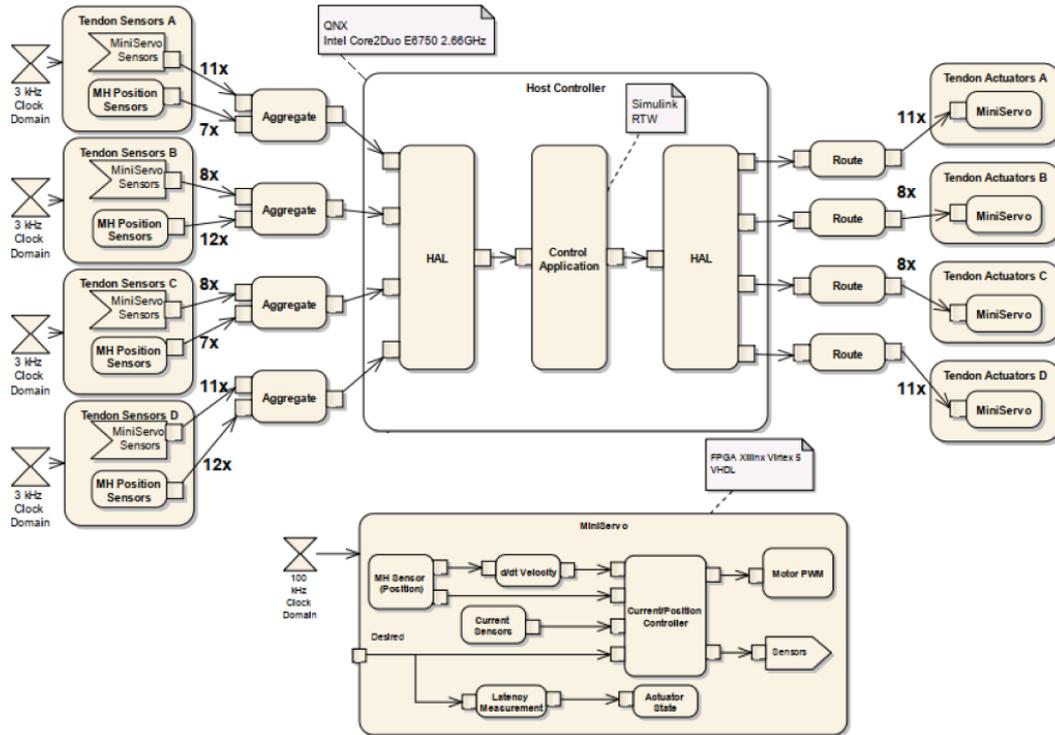


Figure 2.17.: DLRHAS Hand Controller Architecture [Gre+11]

Due to the complexity of the hardware system, the DLRHAS implements the "Virtual Path" component model [JNH09] to tackle the challenges associated with distributed systems and also provides a HAL to provide developers convenient and direct access to all of the robot system functionality. The HAL is implemented with *Matlab Simulink* and provide all relevant signals as SI-Units to the user based on the framework proposed by [JNH06]. This approach allowed for efficient integration of the distributed heterogeneous electronic components while maintaining synchronisation. A simpler architecture was also employed for the *CyberTUM* prosthesis and both systems rely on connectivity with a high-level computational unit responsible for high-level control. This approach suits the experimental nature of the two platforms and simplifies the development and testing of high-level control strategies.

DLRHAS	
<b>Motors</b>	52 (BLDC)
<b>Transmission</b>	Harmonic Drives & Tendons
<b>DOF</b>	26 (19 in hand, 2 in wrist, 5 in the arm )
<b>Mechanism</b>	Hyper-Actuation variable compliance system
<b>Feedback</b>	Joint/Motor Position, Joint Stiffness
<b>Sensors</b>	Angular Position, potentiometer (compliance mechanism), Current, Voltage, Temperature
<b>Max Grip strength</b>	Power (N/A), Precision (30N)
<b>Communication</b>	Spacewire (inter controller), BiSS(sensors)
<b>Control Strategy</b>	Distributed with Hardware Abstraction Layer (HAL)

Table 2.5.: DLRHAS key specifications

### 2.4.3. State-of-the-Art Summary

Specification	MSRM	SHS	BBH	SH2-P	DLRHAS
<b>Motors</b>	2 (BLDC)	2(DC)	2(DC)	5(DC)	52 (BLDC)
<b>Transmission</b>	Harmonic Drives & tendons	N/A	Bespoke linear actuators	Planetary Geartrain & tendons	Harmonic Drives & Tendons
<b>DOF</b>	3	2	6	20	26
<b>Mechanism</b>	Tendon Based with compliant gripper	Tri-digit C-shape	Synchronous	Tendon Based adaptive under-actuation	Hyper-Actuation variable compliance system
<b>User Interface</b>	EMG, Smartphone App, FSR	EMG	Button & EMG	EMG	High level Control PC
<b>Feedback</b>	Relative Motor Position, FSR force measurement, PR tactile sensing for object recognition	Thumb & Grip Force Sensor	Fingertip force sensor, EMG	Tendon Position and Force	Joint/Motor Position, Joint Stiffness
<b>Sensors</b>	FSR (10 Ch), IMU, EMG (2 Ch)	Velocity sensor & Force Sensors	Position, current sensors	Position, current sensors, EMG 2-Ch (Competition) 8-Ch Research)	Angular Position, Potentiometer (compliance mechanism), Current, Voltage, Temperature
<b>Max Grip strength</b>	Not Measured	High (100N)	Power (75N), Precision (35N)	Power (76N), Pinch (20N)	Power (N/A), Precision (30N)
<b>Communication</b>	EtherCAT (1kHz)	N/A	Bluetooth	Serial (RS485)	Spacewire, BiSS
<b>Control Strategy</b>	Distributed with HAL	Centralised	Centralised	Centralised	Distributed with HAL

Table 2.6.: Summary of all devices reviewed

## 2.5. Electronics Platform Feature Selection

This section focuses on the selection of the desirable features and functions found on the state-of-the-art devices evaluated and addresses the limitations identified with the current *CyberTUM* prosthesis. The features selected form the design basis and requirements of the more capable electronics platform for future students to develop the next generation of the *CyberTUM* prosthesis.

### 2.5.1. Degrees of Actuation

Independent operation of each **DOF** in a manner similar to the human hand would require several actuators which increases complexity and is difficult to achieve within the dimensional constraints imposed by the application. It is therefore necessary to reduce the number of actuators used while maintaining as much functionality as possible.

As the mechanical design, mechanism selection and desired hand kinematics lie outside the scope of this thesis, the electronics platform needed to be designed with flexibility and expansion in mind to support future device configurations. The limitations identified with the two actuator solution of the current design indicated that there was room for improvement by redesigning the mechanism. As such, the number of actuators to support was a key design parameter for the electronics platform proposed.

### Hand Mechanism

The decision to support either a *synchronous* or *adaptive* mechanism can be condensed to a decision on how many actuators to support. The simplicity of an *adaptive* under-actuated tendon based mechanism was favoured as it provides the best compromise between complexity and performance. This choice also help achieve lower weight due to fewer actuators and supporting electronics. However, more advanced control techniques are required due to the more complex interaction between joints and the object being grasped and the number of **DOF** controlled by each motor. Finally, a trade-offs is also required in the grip forces achievable due to the inefficiencies introduced by tendon friction forces which needed to be overcome with fewer actuators.

This decision was reinforced by a recent study of mechanical designs of research and commercial prosthetic devices by [Sem+19], which suggests that adaptive tendon based mechanisms are gaining traction. The study [Bel+13] highlights the relationship between achievable **DOF** and the number of actuators utilised, but as previously established, not all are necessary to perform the majority of **ADL**.

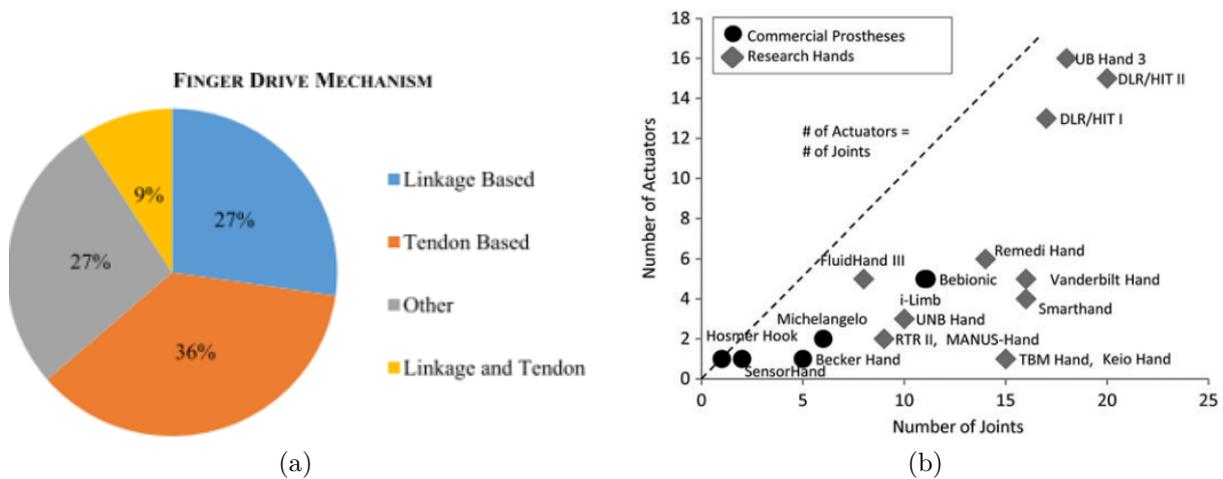


Figure 2.18.: (a) Trends in actuation configuration [Sem+19] (b) Trends in DOA vs DOF correlation [Bel+13]

As previously established, the human thumb features five **DOF** and according to [BM92], the thumb accounts for 40% of hand functionality. Because of the significant contribution to overall hand functionality and importance for completing many **ADL**, the majority of commercial and research designs implement either a passive or active thumb. Owing to the complexity of the human thumb, the majority of devices reviewed feature a simplified one or two **DOF** thumb mechanism driven by a dedicated actuator. Based on these findings, at least two actuators need to be dedicated to powering an under-actuated adaptive mechanism required to realise functionality of fingers and a thumb of a future prosthesis.

### Importance of the Wrist

The human wrist features two **DOF** with a third provided by the forearm. The most commonly used degree of freedom is *pronation/supination*, followed by *flexion/extension*. Finally, *radial/ulnar* deviation is used least frequently and is often viewed as the least important [SR+90] and omitted from most designs.

Functional wrist motion is important for reducing bio-mechanical strain on the user and studies have shown that without a wrist, amputees are forced to compensate with unnatural movements to complete standard **ADL** [Car+08], as shown in Figure 2.19. The results of the study suggest that the combination of wrist with *flexion/extension* and *pronation/supination* and a prosthetic hand allows the patient to perform motion patterns of daily life more naturally.

Historically, significant research effort has been focused on increasing the number of **DOF** in the hand. However, the study by [MCC15] reveals that the importance of the wrist must also be considered. The existing *CyberTUM* prosthesis featured an actuated wrist allowing for *flexion/extension* as well as *pronation/supination* near the elbow with a manual rotation and locking mechanism. The addition of active rotation capability would have been particularly helpful for tasks such as the cup stacking and light bulb screwing task.

The manual rotation and locking mechanism proved to be cumbersome and unpopular with

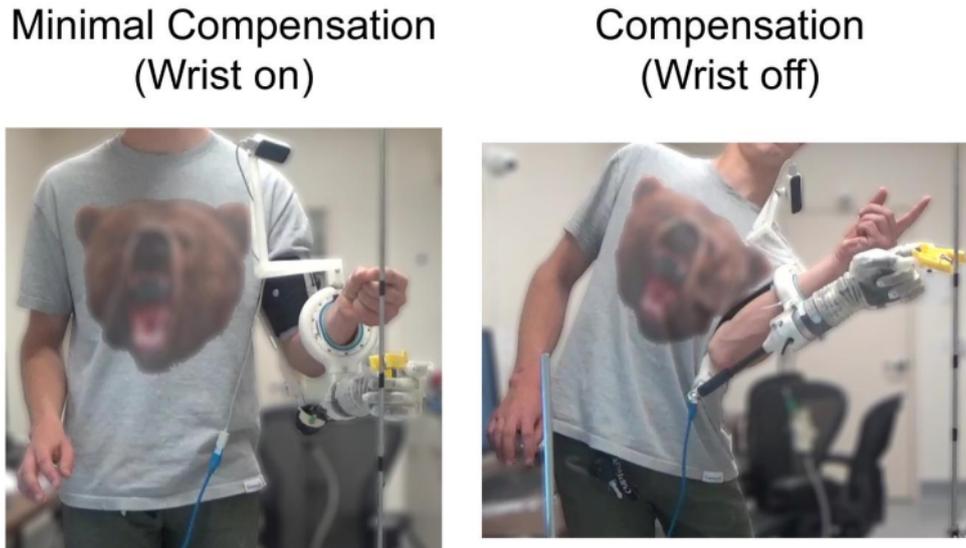


Figure 2.19.: Task comparison with and without active wrist compensation [Ols+19]

the pilot and replacement with an active joint would further enhance functionality. Based on these findings, the platform design proposed needed to support an additional two additional actuators to control the wrist *flexion/extension* and *pronation/supination*.

### Selection Summary

In summary, based on the review performed in the previous section the goal was set to provide a platform with support for at least four actuated **DOF**. A configuration consisting of a 2-DOF hand and 2-DOF wrist was envisaged to provide the right compromise between prosthesis weight, size and complexity while providing sufficient functionality for the most common activities of daily living. This configuration can easily be adapted to suit different applications and highlights the flexibility possible with the platform proposed.

### 2.5.2. Supported Motors

The benefits of **BLDC** motors over traditional brushed **DC** was established and the platform design aimed to support **BLDC** motors to capitalise on the inherent power-to-weight advantage that is so critical in a prosthesis application. The additional complexity introduced by the electrical commutation was solved easily by using motors with integrated Hall sensors. The experience necessary to implement a **BLDC** based design was already gained with the *CyberTUM* prosthesis.

An additional benefit of developing hardware able to drive **BLDC** motors, was that the same hardware could be used to also drive **DC** motors, with only minor software changes required. This flexibility meant that the platform could be used to drive either motor type, should the need for it arise in the future.

### 2.5.3. Controller Architecture

The majority of commercial and research prostheses reviewed in the previous section implemented a centralised control. With this approach, all the sensors and actuators are connected directly to a central controller which handles all the required processing. As such, no communication bus between controllers is required. This approach is feasible for the relatively simple task control state machines based on DC motor control, button based grip selection or on-off and proportional EMG control signals. However, this approach is neither modular nor scalable. Development is also often limited to low-level microcontroller implementation which requires more expertise and development effort. Signal oriented development in environments such as *Simulink* are usually favoured in the research community to develop higher level control systems.

As device complexity increases along with the implementation of computationally heavy algorithms, such as pattern recognition and sophisticated high-level control strategies, the strengths offered by *decentralised* control concepts to offload parts of the computation effort to intelligent low-level controllers become apparent. This concept is demonstrated by the *decentralised* approach used by DLRHAS which features intelligent computation and control nodes internally but the high-level control tasks take place on an external host system. This approach was also used for the *CyberTUM* prosthesis and will be retained due to the flexibility offered, which is important for a experimental research and development platform.

### 2.5.4. Communication Architecture

The DLRHAS also incorporates high-level hardware abstraction which aims for feedback control with cycles beyond  $1kHz$  which are necessary for control performance. Various common research platforms were reviewed by [Syg+01] which used legacy field bus technologies such as CAN for distributed control of humanoid robots. The findings showed that update rates were limited to below  $500Hz$ , and in some cases, multiple parallel networks or modified versions of CAN were required to achieve update rates approaching  $1kHz$ . Also noteworthy, CAN does not compensate for transmission delay and is not entirely deterministic due to message arbitration and bit stuffing.

*EtherCAT* was previously used successfully for the *CyberTUM* prosthesis and the need to transfer real-time control and sensor data between high-level host controller and intelligent low-level modules remained. As such, *EtherCAT* communication was retained for this platform due to the  $100Mbit/s$  bandwidth, cycle times as low as  $100\mu s$  and the distributed clock synchronisation mechanism.

[Zha+15] and [Syg+01] were able to achieve cycle rates in excess of  $4kHz$  and slave synchronisation with  $3.25\mu s$  when accounting for propagation delays and slave dependant latency's with the distributed clock mechanism. This level of performance is comparable to the performance of the DLRHAS which relies on a combination of *Space-wire* and *BISS* interfaces. Interfaces traditionally integrated into microcontrollers used for data exchange between controllers such as CAN, UART and RS-422/485 were not sufficient for this application. Therefore, the additional hardware required to communicate with the *EtherCAT* was incorporated into the design.

### 2.5.5. HMI

Due to widespread adoption and potential as a primary control mechanism, sEMG was selected as the primary control input method for this electronic platform. As such, the required hardware and software to enable future users of this platform to implement sEMG as the primary control method needed to be provided.

### 2.5.6. Additional Sensors

The current *CyberTUM* prosthesis also included several additional sensors which were necessary to complete competition tasks. The newly introduced haptic box challenge required a solution for the non visual classification of objects of different shapes and densities. The solution adopted by the team used the signals from an array of FSR type sensors embedded in the gripper as an input to a pattern recognition system. This system was able to detect the subtle differences in force distribution caused by the different objects. While it is unknown if the haptic box will be present in the *CYBATHLON 2024 Competition*, the inclusion of an improved signal conditioning for these types of sensors was deemed as necessary to allow for an improved implementation in the future. The same types of sensors were also commonly used to provide force feedback in various applications.

The inclusion of an IMU was deemed important. In addition to the current use-cases, where the IMU was used to implement automatic wrist levelling and pilot assistance during tasks such as cup stacking, new functions such as gesture recognition could potentially be implemented. As such the IMU was retained for the new platform design.

# 3. Preliminary Analysis of Microcontroller Performance

The first step in the development of the overall electronics platform was evaluation and selection of the microcontroller. To do this, preliminary development hardware was selected from a range of evaluation boards provided by [MIRMI](#). The development hardware provided a head start and shifted the focus to firmware development in order to better understand the various performance requirements related to tasks, such as motor control and *EtherCAT* communication.

Following the discussion of the selected development platform, the underlying theory for [BLDC](#) motor control and preliminary results are presented. These results feed into the final platform design by providing a benchmark of the overall resource utilisation and provide concrete data on the capabilities of the selected microcontroller.

## 3.1. Predefinitions & biases

This section provides an overview of factors which influenced component selection and design decisions.

- Microcontroller selection was limited to the *Atmel/Microchip* [MCU](#) range due to prior experience and familiarity, a range of evaluation boards were readily available at the [MIRMI](#).
- The in-house *EtherCAT* hardware and software library was provided by the [MIRMI](#) to limit the scope of work required and reduce development time.
- A range of *Faulhaber BTX* series [BLDC](#) motors were provided for prototyping and development activities.

### 3.2. Microcontroller

The choice of microcontroller is strongly influenced by the desired features and functionality specified for the electronics platform. There are a vast array of controllers available with differing features, integrated peripherals and capabilities. The specific product ranges offered by suppliers usually target common applications and thus certain parts provide features and peripherals more suited to tasks such as motor control. However, datasheet specifications of a microcontroller family are only part of the overall selection process. Other important aspects to consider include prior experience, parts availability, community support and the quality of development tools provided.

A high level summary of the product range and target applications sectors of the *Atmel/Microchip SAM* series of 32-bit micro-controllers is provided in [Figure 3.1](#)

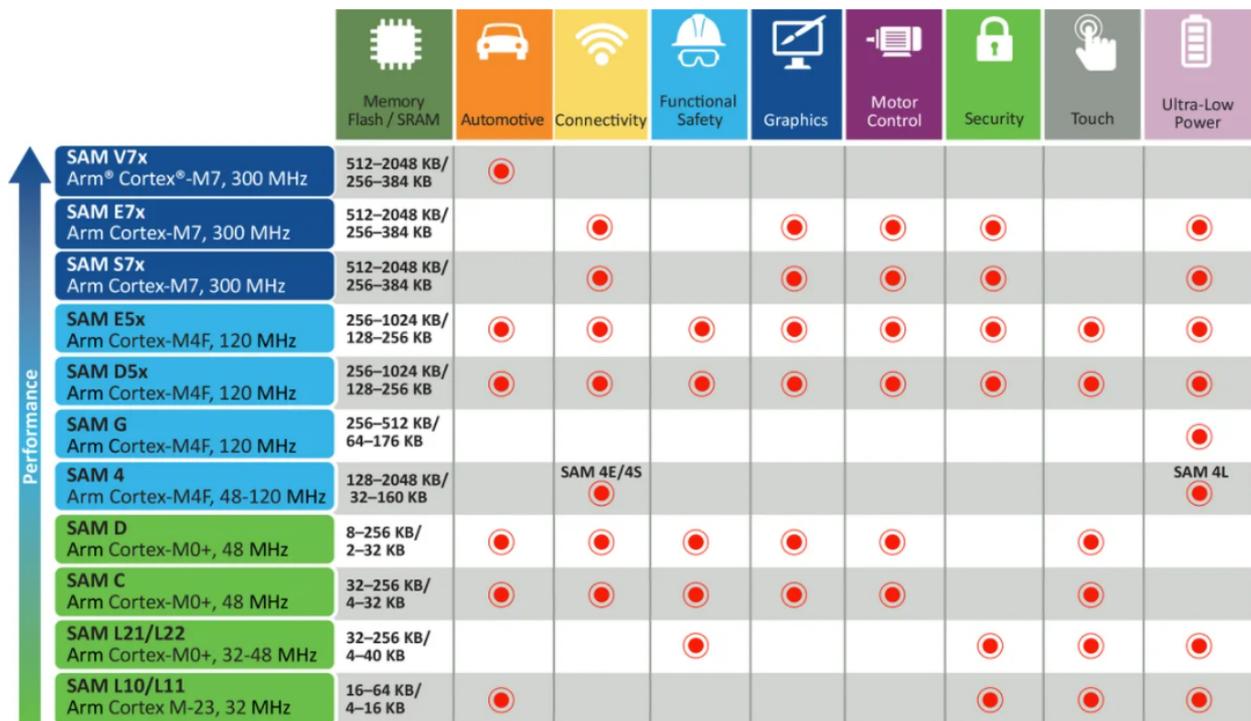


Figure 3.1.: 32-bit SAM Microcontroller family

Members of the *SAM* Microcontroller family from different performance levels listed in [Figure 3.1](#) were evaluated and compared as shown in [Table 3.1](#). The *ATSAMC21* series was used for the previous *CyberTUM* prosthesis and was familiar. During prior development work, the lower clock frequency and lack of hardware *FPU* provides limited head room for further improvement especially with more sophisticated control algorithms.

At the top of the range, the *ATSAME70* provides significantly faster processing performance due to the higher clock frequency and M7 processor core. However, the peripherals provided are different from the *ATSAMC21* and *ATSAMD51*. Additionally, the most compact and desirable 64-pin version of the microcontroller is missing several key hardware features such as *QSPI* and has a limited number of serial communication peripherals and analogue channels

compared to the higher pin-count versions. The mid-range *ATSAMD51* is a new addition to the product range and offers many improvements over *ATSAMC21* but still shares the majority of peripherals. This was significant as the majority of the software previously developed for the *CyberTUM* prosthesis can be easily adapted or reused.

Parameters	ATSAMC21	ATSAMD51	ATSAME70
<b>Operating Voltage(V)</b>	2.7-5.5	1.7-3.6	1.7-3.6
<b>Max Clock Freq(MHz)</b>	48	120	300
<b>Arm Cortex Core</b>	M0+	M4	M7
<b>Floating Point Unit</b>	No	Yes <sup>1</sup>	Yes <sup>2</sup>
<b>Max Program Memory (kB)</b>	256	1024	2048
<b>Max SRAM (kB)</b>	32	256	384
<b>Pin Counts</b>	32,48,64,100	48,64,100,128	64,100,144
<b>Packages</b>	QFN,TQFP	QFN,TQFP,BGA	QFN,TQFP,BGA
<b>ADC Count</b>	3	2	2
<b>Max ADC Resolution(bits)</b>	12	12	12
<b>Max Sampling Rate (ksps)</b>	1000	1000	1700
<b>DMA Channels</b>	12	32	24
<b>Max Serial Interface</b>	8	8	3 (USART)+2SPI
<b>QSPI Support</b>	No	Yes	Yes <sup>3</sup>
<b>Official Development Board</b>	Yes	Yes	Yes
<b>Available@MIRMI</b>	Yes	Yes	Yes
<b>Available(Des. Time)</b>	Yes	Yes	Yes

<sup>1</sup> Single Precision

<sup>2</sup> Double Precision

<sup>3</sup> Not available on 64-pin version

Table 3.1.: MCU Family Selection Shortlist

The higher clock speed and built-in FPU of the *ATSAMD51* lend themselves to executing control tasks with minimal impact of using floating point instead of fixed point math optimisations. The additional RAM and DMA channels and dedicated QSPI hardware help improve performance and flexibility over the *ATSAMC21* used previously. The specific implementation and controller performance was determined in subsequent sections.

### 3.3. Development Setup

By combining an off the shelf *SAM E54 Xplained Pro* evaluation board, with expansion boards providing the necessary motor control, and *EtherCAT* hardware provided by *MIRMI*, all the hardware necessary for initial firmware development and testing was established as shown in *Figure 3.2*. *SAM E54 Xplained Pro* is the only official development board available in the *SAMD/E51* family and features the *ATSAME54P20A* microcontroller, the most feature rich microcontroller in the family with a 128-pin package. While this differs from the more desirable space efficient 48 and 64 pin packages, the extra *GPIO* pins and debugging features available are ideal during development.

The standard *Microchip* tool-chain, including *Microchip Studio*, the *Atmel Start* configurator and associated *ASF4* driver, and middleware framework were used for firmware development. *EtherCAT* communication requires a dedicated master to initiate communication and configure the attached slave devices, for this a standard *Windows PC* and *TwinCAT 3.1* was used for all development.

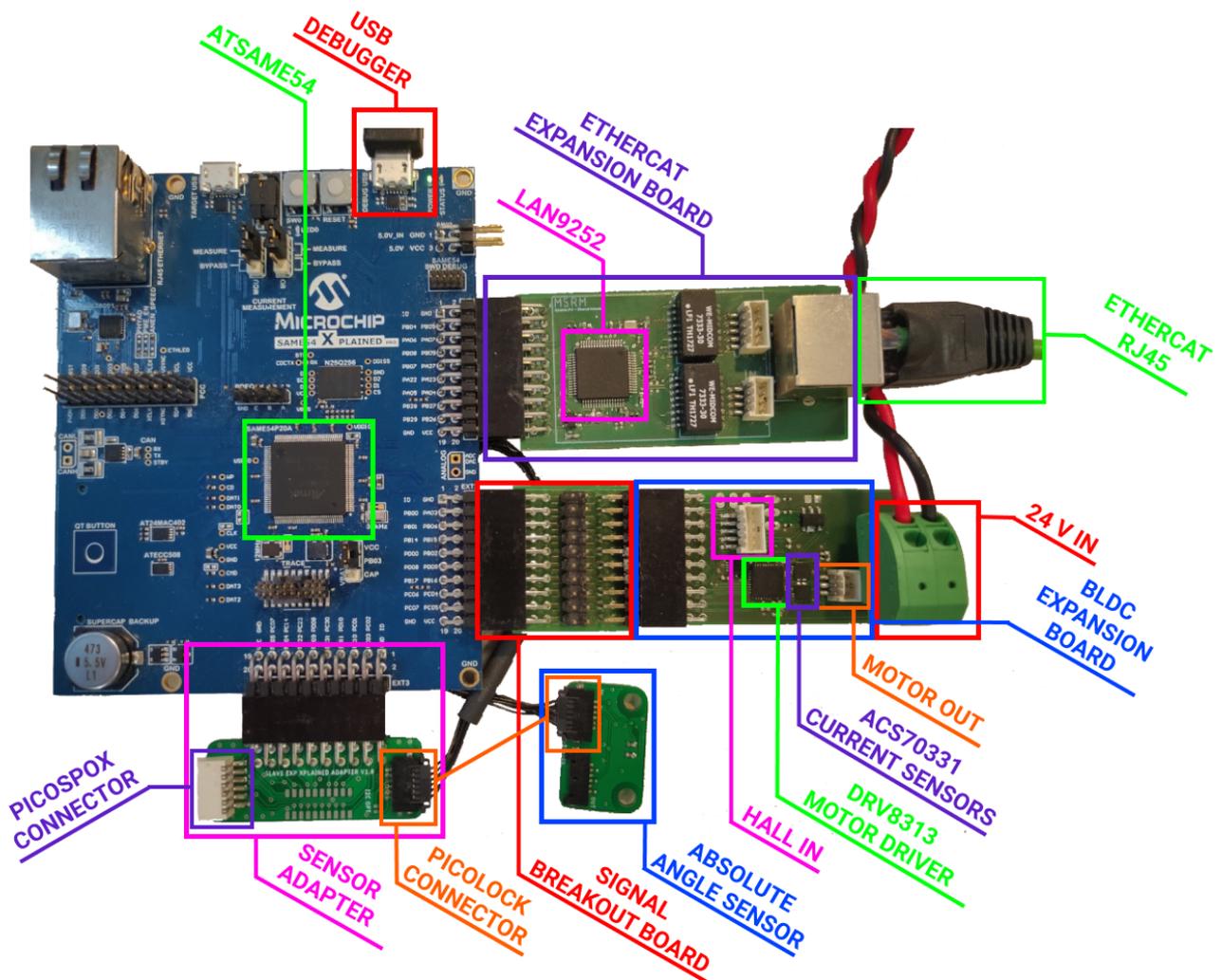


Figure 3.2.: Development Setup

### 3.3.1. Block Diagram & Functionality

A block diagram for the development platform is presented in [Figure 3.3](#) and provides an overview of the components, signals and microcontroller peripherals involved to develop and test the motor control and communication firmware and establish preliminary results on performance and computation resource requirements. This structure is an evolution of the implementation used in the original *CyberTUM* prosthesis and includes improvements such as cascaded control identified in [chapter 2](#).

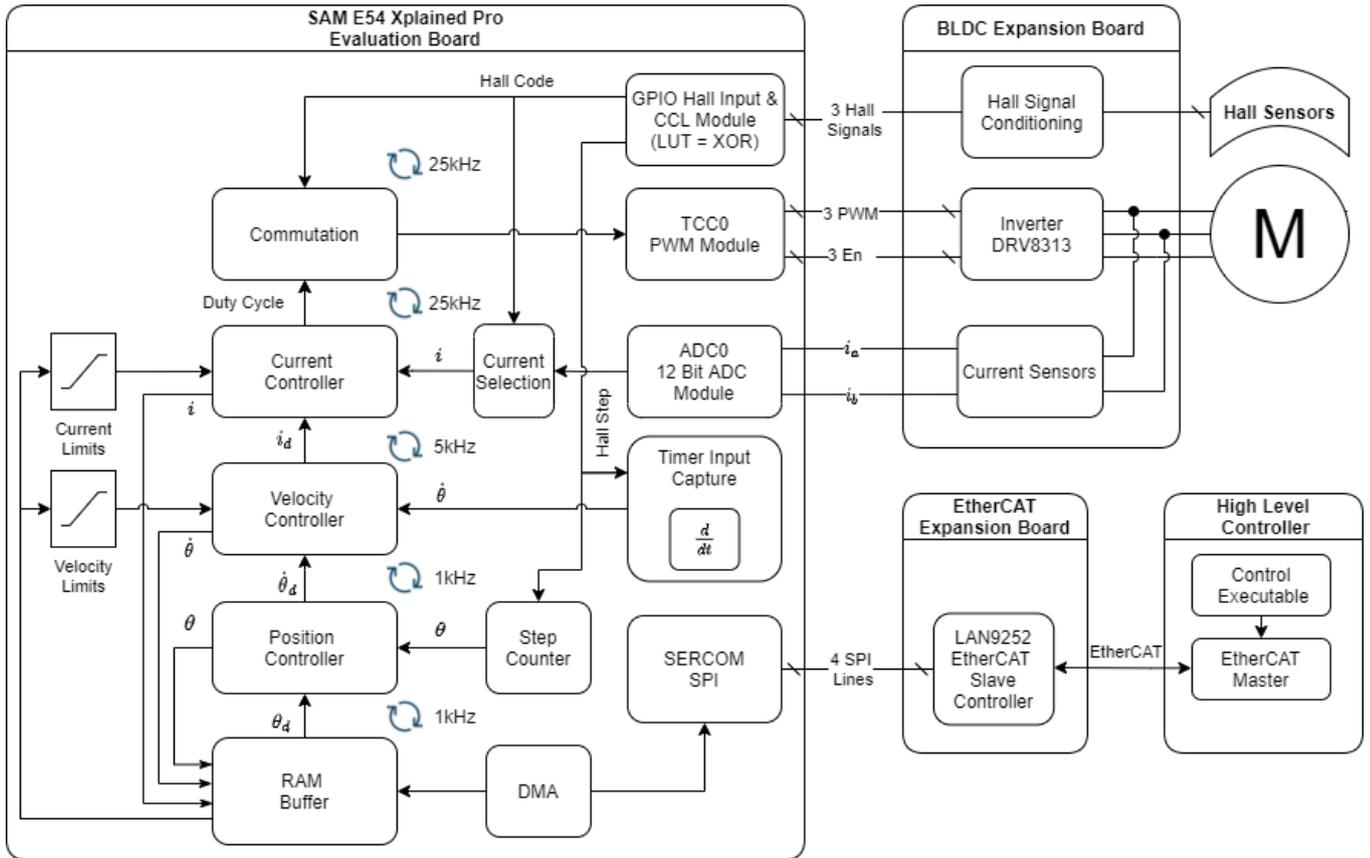


Figure 3.3.: Development Block Diagram

#### EtherCAT Interface

*EtherCAT* is an *Ethernet* based communication protocol that maintains short cycle times, low latency and features a built-in synchronisation mechanism. In order for devices to communicate, an *EtherCAT Master* is required to initiate transfers and configure the attached *slave* devices. Every *slave* device must contain an *EtherCAT* specific ASIC, known as the [EtherCAT Slave Controller \(ESC\)](#), which is responsible for all *EtherCAT* related data processing.

The [MIRMI](#) institute uses *EtherCAT* extensively in research activities and has developed hardware modules and software libraries for *Microchip LAN9252* series of [ESC](#). The hardware was provided and closely follows the reference implementation provided by [[Mic16](#)] and communicates with the host controller on the *SAM E54 Xplained Pro* via SPI as shown in [Figure 3.3](#).

The required software library was also provided and was largely used as is. The implementation was adapted to the new processor platform and uses **DMA** to perform cyclic data transfers between *RAM* based buffers in the host microcontroller and **ESC**. This is significant as communication occurs in the background, without intervention or overheads, allowing the processor to focus on control related tasks. The specific library implementation details are considered out of the scope of this thesis.

### Motor Control Hardware

The transistors bridges necessary to control the 3-phases of the **BLDC** motor need to be precisely controlled by a microcontroller. Microcontrollers are not capable of sourcing the required current to effectively drive these transistors. The expansion board provided by **MIRMI** contains the necessary driver to control the supplied *Faulhaber 3216W024BXTR* **BLDC** motor from the *SAM E54 Xplained Pro* evaluation board. The board features a *DRV8313* motor driver IC with integrated **MOSFETs** in a triple half bridge configuration and is responsible for delivering the 24 V power to the three phases of the **BLDC** motor with a **Pulse-width modulation (PWM)** voltage. Inline *Allegro ACS70331* current sensors are provided on two of the three phases as the third phase current can be derived from the two other phases. Finally, the board also provides the necessary connectors for the 24V operating voltage, motor and integrated hall sensors.

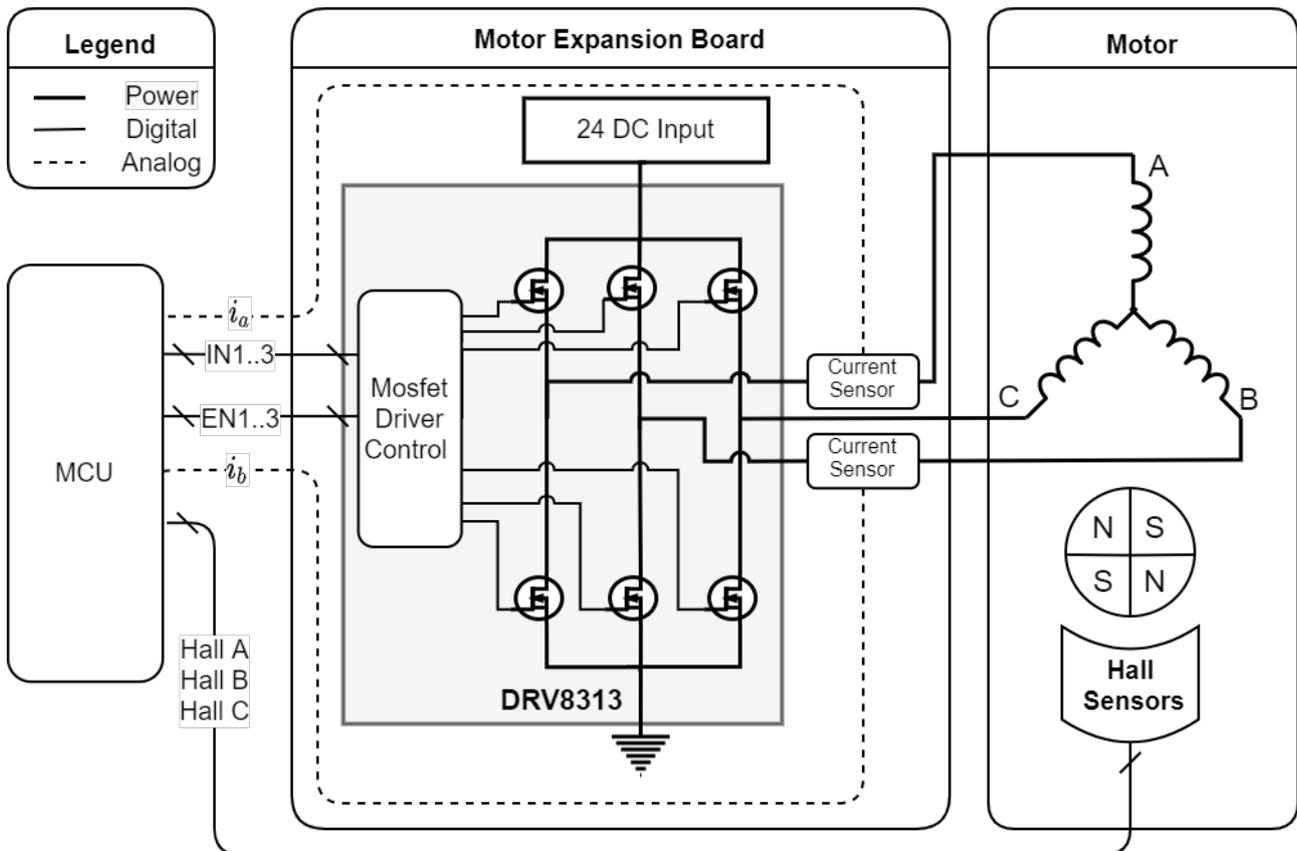


Figure 3.4.: BLDC Motor Control Hardware

## 3.4. Motor Control

In order to implement a controller for Brushless permanent magnet motors, it is important to understand their construction and established control methods. Brushless motors can be categorised in terms of the shape of the back-EMF waveform they exhibit. Motors with a sinusoidal shape back-EMF are commonly referred to as [Permanent magnet synchronous motors \(PMSM\)](#) and motors with a trapezoidal shape back-EMF are known as [Brushless DC \(BLDC\)](#) motors. This distinction is important when selecting the control technique to be used. Both motors are powered by a DC source and electronically commutated, the difference is related to the construction of the stator windings.

The windings of the stator must be energized in the correct sequence based on the position of the rotor in a process known as commutation in order for the motor to rotate. In this section, a brief overview of common commutation methods is presented, the selected [Six-step Commutation \(6SC\)](#) is explained and the cascaded controller theory is outlined. Finally, preliminary controller performance and microcontroller resource requirement results are presented. These results were used as the basis for the final electronics platform controller selection.

### 3.4.1. Commutation Methods

The shape of the back-EMF behaviour does serve to make each individual motor more suited to, but not limit, a particular commutation method. The most widely used and simplest technique to control [BLDC](#) motors is [Six-step Commutation \(6SC\)](#). [PMSM](#), on the other hand, are commonly controlled using sinusoidal commutation or [Field-oriented Control \(FOC\)](#). Sinusoidal commutation replaces the flat peak of the trapezoid with a sinusoidal waveform that matches the back-EMF more closely. [FOC](#) enables separate control of electromagnetic torque and magnetising flux of the motor [[ZVM52](#)].

An illustration of the effect of the chosen commutation method on both types of motors is shown in [Figure 3.5](#). The results presented by [[Sum+19](#)] highlight the peak torque differences as well as the torque ripple induced due to the non-ideal interaction of the back-EMF and phase current harmonic components when using [6SC](#) on a [PMSM](#) and [FOC BLDC](#), respectively. The torque ripple inherent in [6SC](#) is due to the non-linearities in the commutation scheme as only two motor phases being energised at any given time is not shown and is more pronounced at lower speeds.

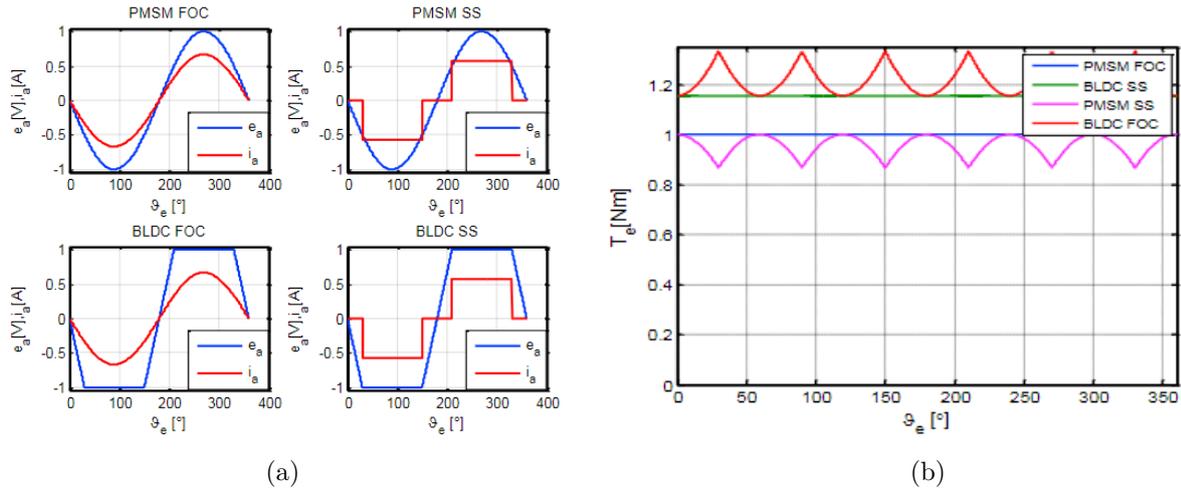


Figure 3.5.: (a) Comparison of ideal motor back-emf and phase current input waveform. (b) Resultant torque vs rotor position [Sum+19]

A summary of the characteristics of the three methods is provided in Table 3.2.

Commutation Method	Speed Control	Torque Control		Required Feedback Devices	Algorithm Complexity
		Low Speed	High Speed		
Trapezoidal	Excellent	Torque Ripple	Efficient	Hall	Low
Sinusoidal	Excellent	Excellent	Inefficient	Encoder	Medium
FOC	Excellent	Excellent	Excellent	Current Sensor, Encoder	High

Table 3.2.: Commutation Schema Comparison [LLK09]

Given the analysis of available motor commutation methods and the knowledge that the *Faulhaber* motor provided exhibits trapezoidal back-EMF, the decision was made to implement the motor controller using 6SC.

### 3.4.2. Six-step Commutation (6SC)

The name of this technique is derived from the control principle where only two of the three phases are energised at any time. Torque is maximised when the angle between the stator magnetic field and the rotor flux is kept close to 90 degrees [ZVM52]. To achieve this, it is important to know the rotor position in order to understand which winding will be energised next, based on a predetermined sequence. While other higher resolution and even sensor-less rotor position sensing techniques exist, the most common type of sensor used is the Hall effect sensor and the *Faulhaber BTX* series motor provided features integrated sensors.

These sensors detect the rotors magnetic poles and are placed  $60^\circ$  electrical apart, hence there are six unique sensor states per electrical revolution. The actual mechanical spacing is a property of the pole pair count of the motor. Figure 3.6 presents the phase current and back-EMF

sequence based on the Hall sensor pattern and associated sequence number where a positive waveform represents current flowing into the winding, negative flowing out and zero, an open circuit (High-Z) state. This sequence is encoded in the firmware as a lookup-table used to control the appropriate *DRV8313* MOSFETs to commutate the motor based on Hall input signals.

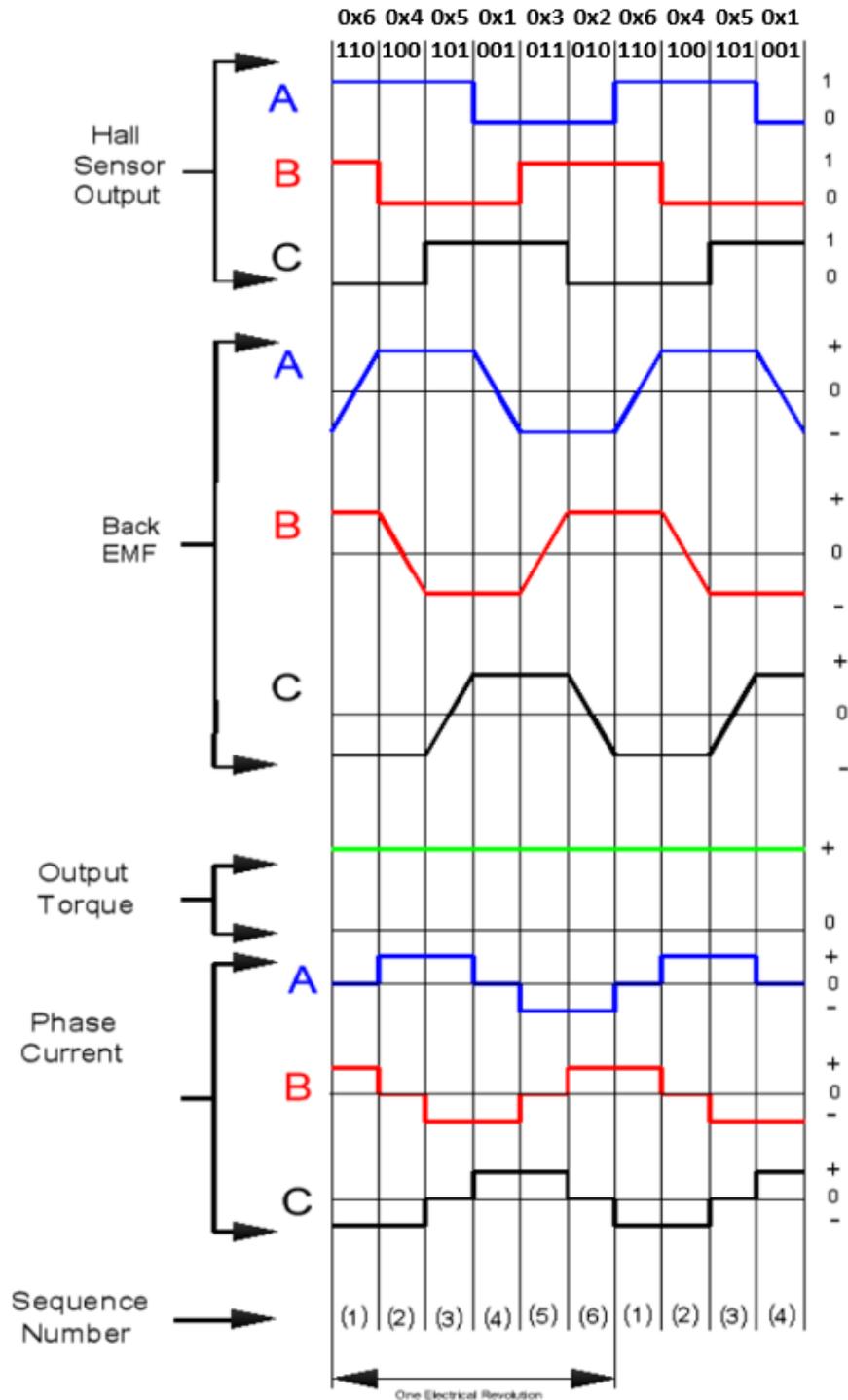


Figure 3.6.: Six-step Commutation (6SC) and Corresponding Motors States [Pad24]

### 3.4.3. Cascaded Control

Prior development efforts for *CyberTUM* prosthesis were limited to position control of a BLDC motor. As an improvement, a cascaded control solution was implemented to allow closed loop control over current/torque, speed and position. The overall controller architecture implemented is shown in Figure 3.7. Several simplifying assumptions regarding the load to be controlled were necessary as the configuration for future prosthetic devices developed using the platform is not yet known. Variables such as load inertia, viscous damping, gear ratios and exact motor parameters are application specific and would require additional tuning effort in the future.

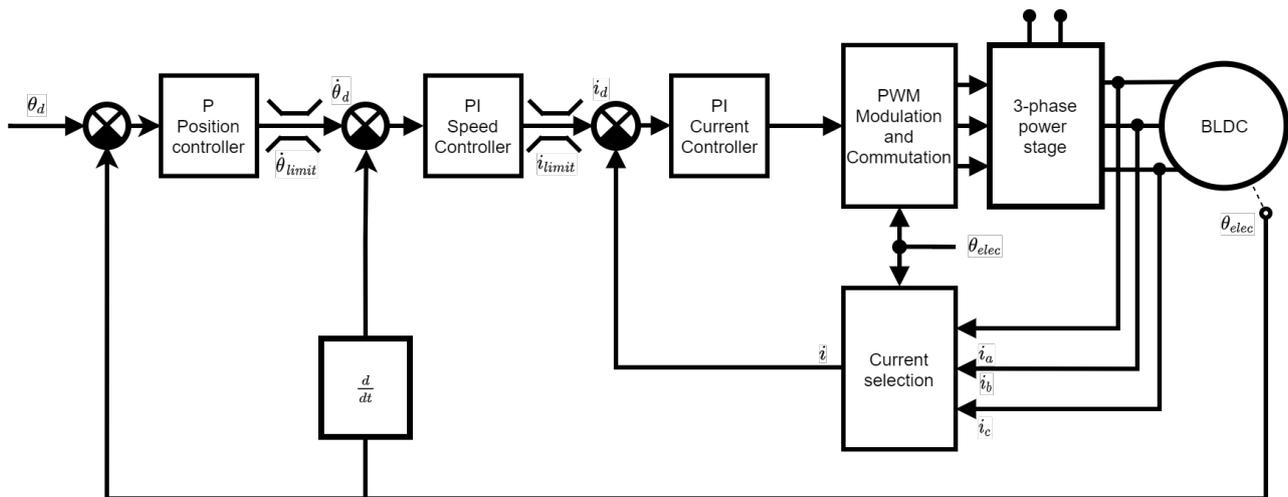


Figure 3.7.: Development Block Diagram

### Current Control

In motor control, one of the the key performance characteristics of these systems is torque response which is directly related to current loop performance, motor torque is proportional to the motor current. The current loop is the linchpin upon which the performance of the rest of the system depends [Bri17]. The current-loop bandwidth is the most critical factor because it influences the ability to respond quickly to load perturbations and dictates the maximum performance of the speed and position loops built on top.

Current controllers are commonly implemented with PI controllers and two general forms exist, the *parallel* and *series* form. The frequency responses are identical, but each form has application specific advantages. The mathematical derivation for each form is presented by [Tex19]. This material was used during the controller firmware development as it provides a wealth of motor control specific information and covers the relevant control theory and implementation nuances and pitfalls.

The torque controller is best analysed as a series PI controller with a first order approximation of the motor winding as shown in Figure 3.8

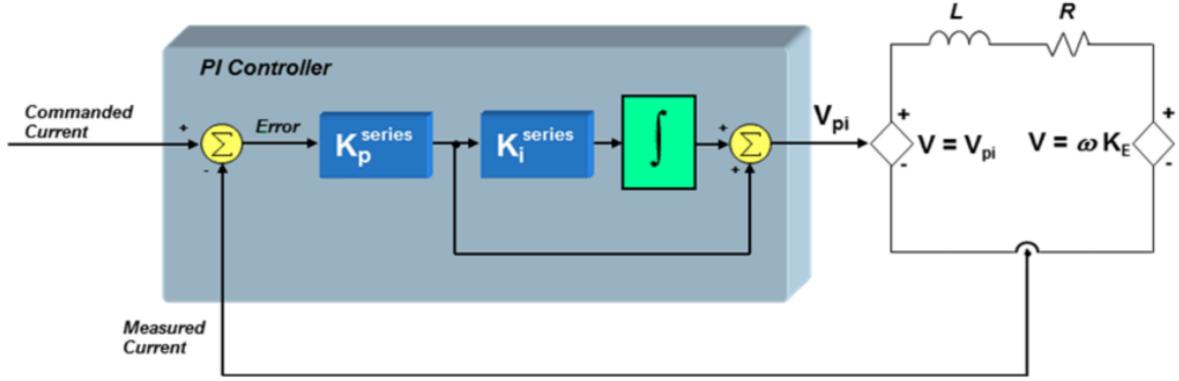


Figure 3.8.: Current Controller Block Diagram [Tex16]

The s-domain transfer function of the series for of the PI controller is given by:

$$PI(s) = \frac{K_p^{series} \times K_i^{series}}{s} + K_p^{series} = \frac{K_p^{series} \times K_i^{series} \left(1 + \frac{s}{K_i^{series}}\right)}{s} \quad (\text{Eq. 3.4.1})$$

From this, it is clear that a pole exists at  $s = 0$  and a zero exists at  $s = K_i^{series}$ . This result is significant in the current controller application. A first order approximation for the motor winding consists of an inductor  $L$ , a resistor  $R$  and a back-EMF voltage source as shown in the figure above. The derived transfer function in the S-domain.

$$\frac{I(S)}{V(S)} = \frac{\frac{I}{R}}{1 + \frac{L}{R}s} \quad (\text{Eq. 3.4.2})$$

The loop gain of the controller is the product of PI controller transfer function and transfer function for the stator coil equivalent circuit:

$$G_{loop} = PI(s) \times \left( \frac{K_p^{series} \times K_i^{series} \left(1 + \frac{s}{K_i^{series}}\right)}{s} \right) \left( \frac{\frac{I}{R}}{1 + \frac{L}{R}s} \right) \quad (\text{Eq. 3.4.3})$$

The closed loop response is given by (assuming that feedback term  $H(s) = 1$ ):

$$G_s = \frac{G_{loop}(s)}{1 + G_{loop}(s)} \quad (\text{Eq. 3.4.4})$$

After some algebraic manipulation and careful substitution outlined in [Tex19] while exploiting pole zero cancellation, the resulting transfer function has in only one real pole and no zeros.

$$G_s = \frac{\left(1 + \frac{s}{K_i^{series}}\right)}{\left(1 + \frac{R}{K_p^{series} \times K_i^{series}} s\right) \left(1 + \frac{s}{K_i^{series}}\right)} \quad (\text{Eq. 3.4.5})$$

Back substitution results in the following important equities for the controller gains explained in more detail by [Tex19]:

$$K_i^{series} = \frac{R}{L} \quad K_p^{series} = L \times \text{Bandwidth}$$

$K_i^{series}$  sets the zero of the PI controller and  $K_p^{series}$  sets the bandwidth of the closed-loop system response. As such, the loop gains and the motor's series impedance and inductance are critical to the performance of the controller. The impedance and inductance parameters are quoted in the motor datasheet, but fine tuning is always required to maximise controller performance.

### Speed Control

The speed controller is cascaded with the current controller and resides in the mechanical domain where time constants are much slower. Analytical solutions to calculate controller gains for the speed controller are also presented by [Tex19]. However, the final mechanical configuration of a future prosthesis is unknown and motor testing was performed without a gearbox or load attached, therefore this level of analysis was deemed as unnecessary. The velocity controller was implemented using the series structure and gains were obtained by manual tuning to achieve an acceptable step response performance and stability.

### Position Control

The position controller was implemented as a simple P controller cascaded with the velocity and current controllers outlined above. This simplification is possible since the velocity is a PI type controller and the final value theorem reveals that there is no position error in the steady-state condition when there is a step change in load torque.

#### 3.4.4. Data Acquisition

For closed loop control, the relevant motor state variables need to be measured either directly or derived indirectly from another state variable. In this case, the positional information is provided by the rotor Hall sensors. This position information needs to be integrated to derive the speed of the motor. Motor current is obtained using the inline current sensors provided.

### Current

Accurate measurement of the phase currents of a BLDC motor is essential for closed loop current control performance. The inline ACS70331 current sensors are based on the Hall effect and can measure bi-directional currents with a high 1 MHz bandwidth. The sensors output an

analogue voltage proportional to the current flowing through the sensor. The sensors feature a 1.5V offset voltage at zero current and the output swings  $\pm 1V$  to the full scale current of 2.5A and sensitivity quoted at  $400mA/V$ . The equation to convert the voltage obtained using using the microcontroller ADC to the measured current value is shown in Eq. 3.4.6

$$I_{measured} = \frac{V_{Sensor} - V_{offset}}{Sensitivity} \quad (\text{Eq. 3.4.6})$$

The timing of the current sampling is important as the sampling needs to take place in the middle of the applied PWM waveform for maximum accuracy as the phase current reaches its average value. To achieve this, a centre aligned PWM modulation scheme was selected and an event is used to trigger the ADC conversion at the top count. The ADC complete interrupt is used to trigger the current loop execution once the readings are ready.

Based on the current Hall sensor code, the current loop must select the current reading of currently conducting phase, according to the commutation table shown in Figure 3.6. This synchronisation between the PWM generation, ADC conversion and current control loop was tested at  $25kHz$ . All control related calculations need to be completed within the PWM cycle period for reliable closed loop performance. The timing details are outlined in Figure 3.9.

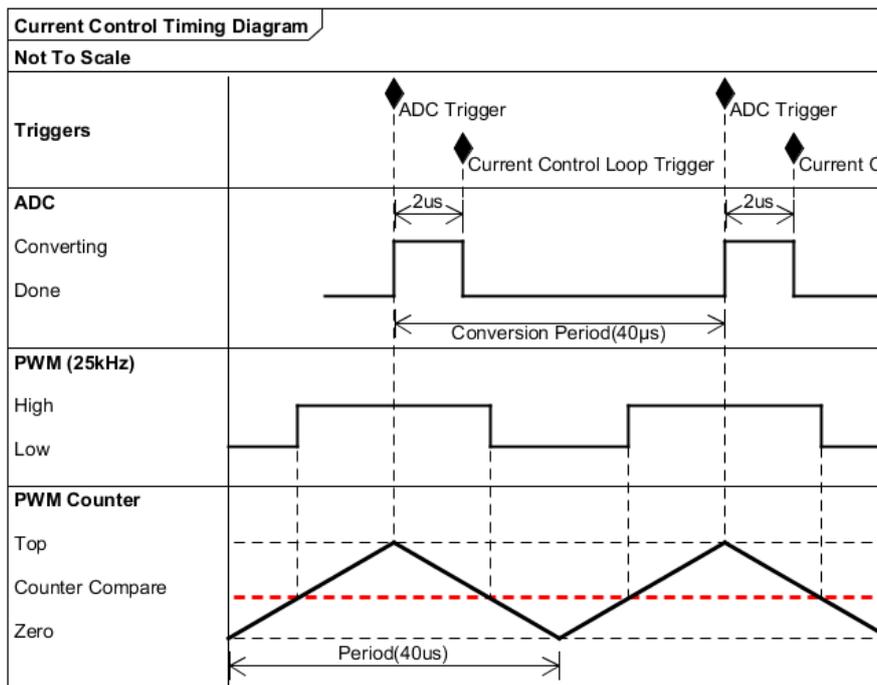


Figure 3.9.: Current Controller Timing Diagram

### Speed (HALL)

Speed feedback is obtained indirectly using the pulses generated by Hall sensors attached to each motor. To improve the resolution and quality of the velocity estimate, the three phase shifted signals from the Hall sensors are fed to the configurable custom logic peripheral (CCL). Traditionally, these logic gates are manually implemented as external components but this feature allows an XOR operation to be performed on the 3 input wave-forms. The resulting waveform is shown in Figure 3.10. The rising edge of this waveform is used to trigger the input capture functionality of a hardware timer. This time measurement represents the pulse width period of a single Hall transition. The speed of the motor is directly proportional to the pulse width captured by the timer. A simple moving average filter is used to provide a clean velocity feedback signal to the controller.

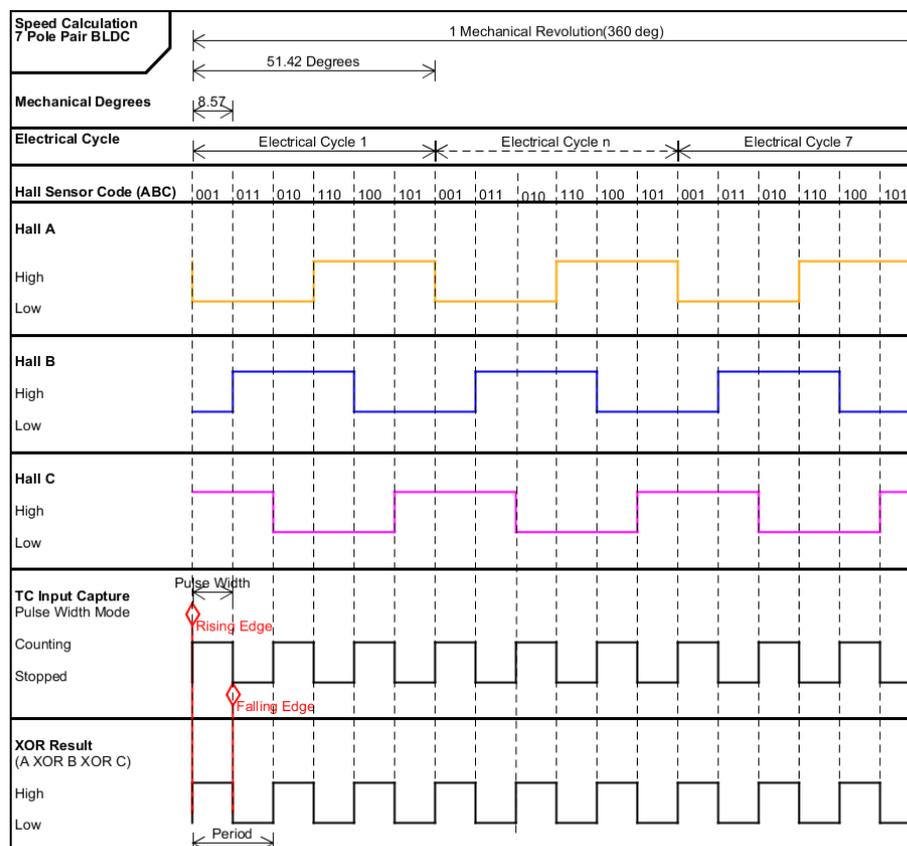


Figure 3.10.: Velocity Controller Block Diagram

### Position (HALL)

Position feedback is obtained by counting Hall sensor step transitions at each commutation cycle. On a 7 Pole motor, these steps occur every 8.5 degrees of mechanical rotation as shown in Figure 3.10. The position feedback obtained from the Hall sensors is of a relatively low resolution; however, most applications would employ reduction gear train between the motor

and the load, as such the relatively low resolution on the driving end would not have as pronounced effect on the driven end. The biggest drawback of this approach is that the position information is relative and the zero position is obtained on startup and lost on power loss.

### 3.4.5. Preliminary Results

The data necessary to analyse the motor control implementation was obtained using an oscilloscope and data streamed over *EtherCAT*.

#### Motor Commutation Waveform

Correct motor commutation can be confirmed by using an oscilloscope. The waveform of each of the motor phases is shown in [Figure 3.11](#). The result confirms that two phases are energised in the correct sequence and that the motor commutation is updated each electrical cycle as required.

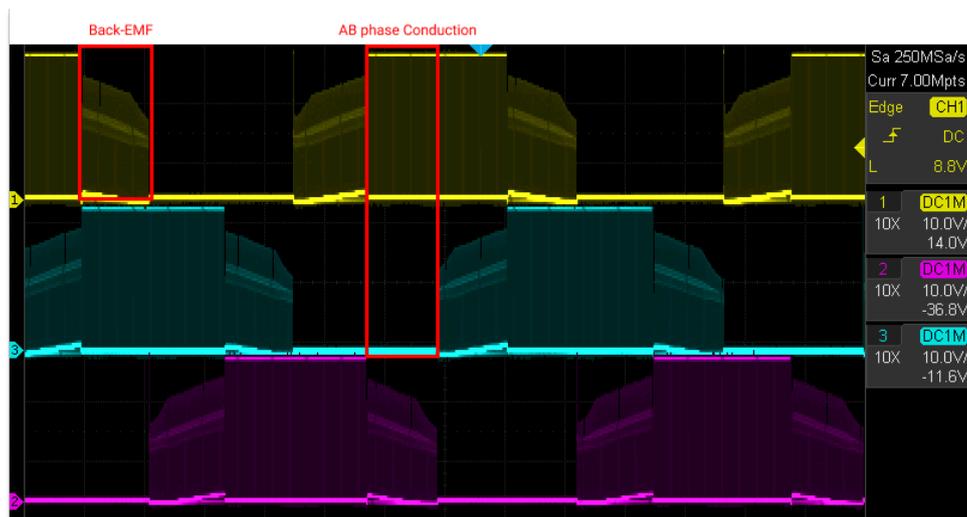


Figure 3.11.: Motor Waveform during Commutation

#### Stalled Current Control

Closed loop current control was verified by stalling the motor and observing current readings. The motor is slowly rotated to confirm that the current selected by the controller matches the currently active phase according to the rotor position. The result for a current step of  $80\text{mA}$  followed by  $110\text{mA}$  step is shown in [Figure 3.12](#).

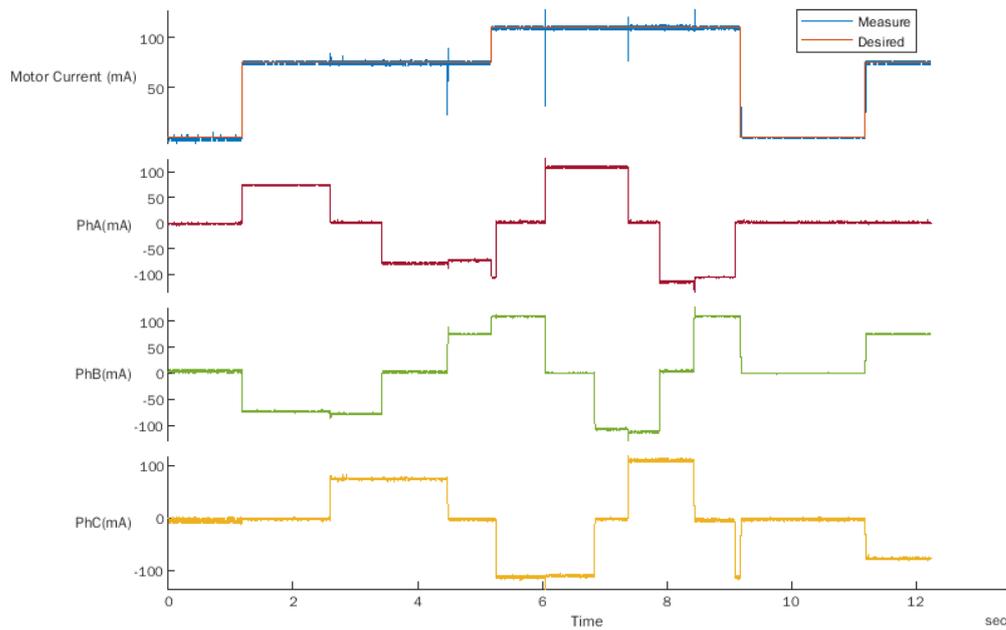


Figure 3.12.: Stalled Current Control

### Current Loop Step Response

The current controller performance was verified using a stalled motor and a  $110\text{mA}$  current step. The response is shown in Figure 3.13. The results confirm that gains derived analytically in the preceding section were acceptable and result in a fast rise time with minimal overshoot and oscillation.

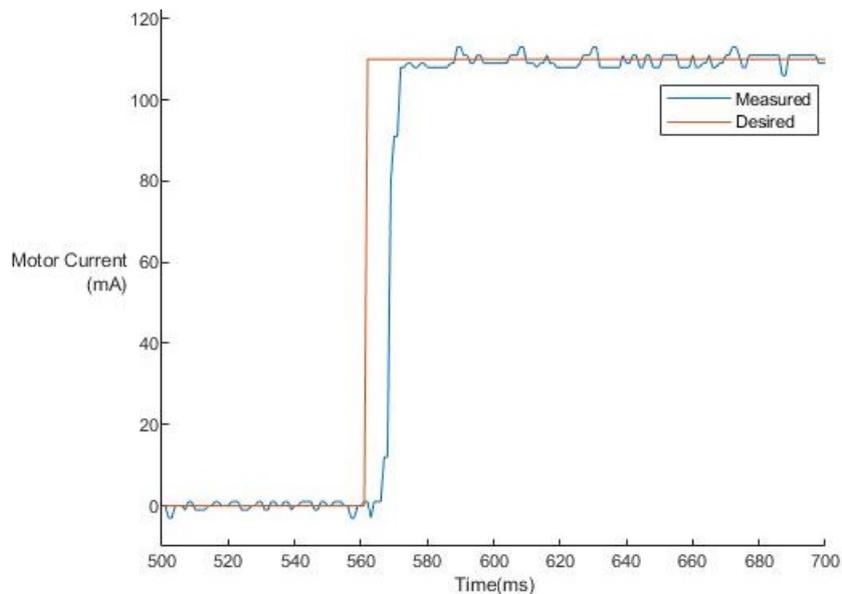


Figure 3.13.: Current Step Response

### Cascaded Controller Response

The remaining velocity and position controller were tuned empirically to achieve a stable response with minimal overshoot and oscillation. The cascaded control response to a series of position set points is shown in Figure 3.14. The response highlights the velocity limits imposed and minimal overshoot achieved.

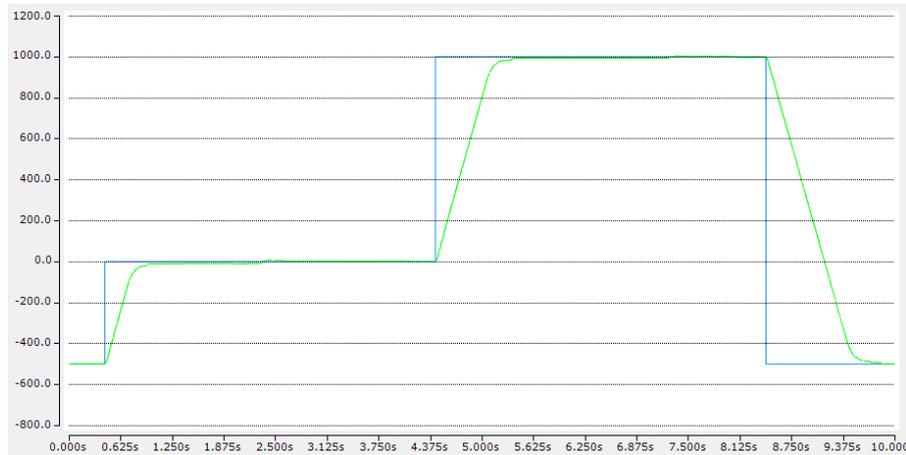


Figure 3.14.: Cascaded controller response

### Resource Requirements

The microcontroller resources required to execute the motor control related tasks was measured using an oscilloscope by setting and clearing dedicated [GPIO](#) pins. The measurements were performed with and without *EtherCAT* communication using the [DMA](#) version of the *EtherCAT* library. The results showed that the timing measurements were not measurably affected. The three control loops execute in different intervals, the worst case result occurs when all three control loops are executed sequentially.

From the data presented in [Table 3.3](#), it is clear that the majority of the control cycle is occupied with the current sampling which is hardware bound, however less than 33% of the processing time is consumed by the motor control task. This result confirms that the PWM and current control frequency could theoretically be increased to increase controller bandwidth and improve motor efficiency, though this may be unnecessary.

The more important result reveals that at least two motors could be accommodated without impacting the desired  $25kHz$  PWM and current loop frequency. Further micro-optimisation may be possible to maximise the remaining processing time for other tasks, but this was found to be unnecessary.

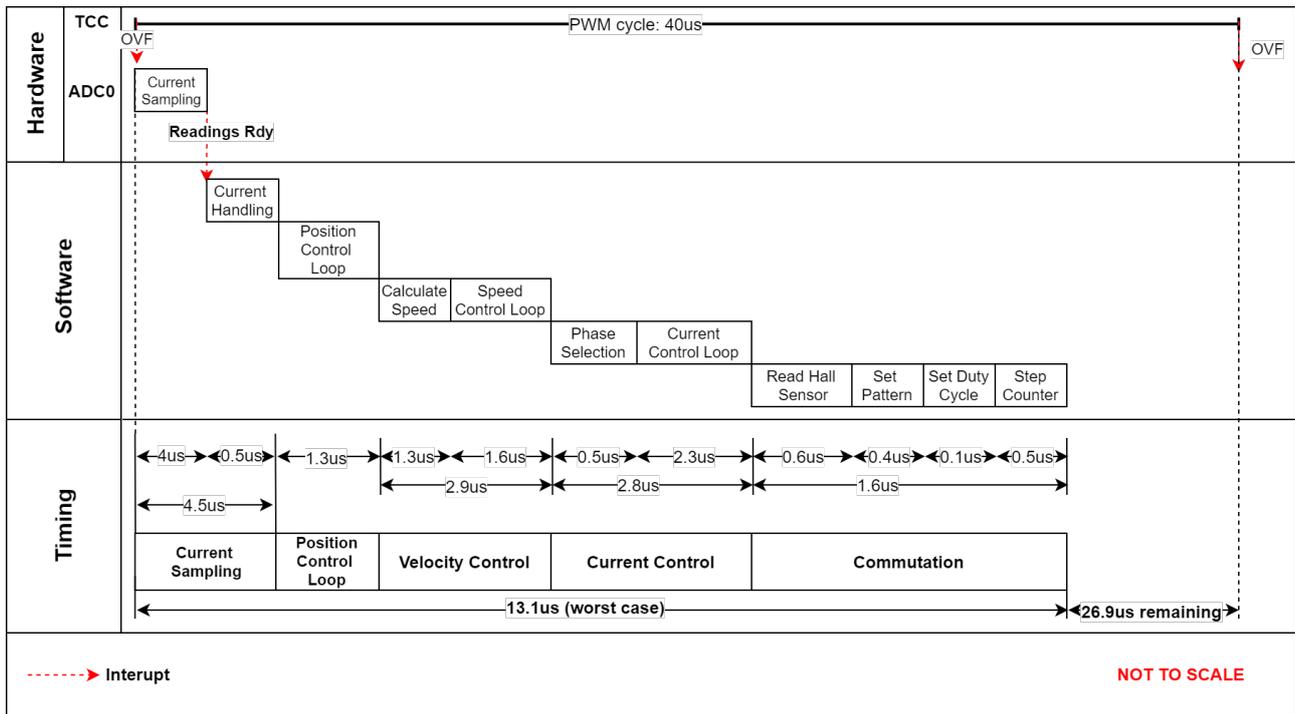


Figure 3.15.: Worst Case Control Execution Timing

Task	Duration (µs)	%	Notes
Current Sampling	4	30.5	2 channel sequence
Current Processing	0.5	3.8	
Position Control	1.3	9.9	Includes Moving average filter
Calculate Velocity	1.3	9.9	
Velocity Control	1.6	12.2	Based on Hall Code
Phase Selection	0.5	3.8	
Current Control	2.3	17.6	
Read Hall Code	0.6	4.6	
Set Driver Pattern	0.4	3.1	
Set Duty Cycle	0.1	0.8	
Increment Step Counter	0.5	3.8	
<b>Total</b>	<b>13.1</b>	<b>32.7</b>	
<b>PWM Cycle Remaining</b>	<b>26.9</b>	<b>67.2</b>	

<sup>1</sup> Percentage Of PWM 40 µs period

Table 3.3.: Worst case Computation time as a percentage of PWM period

## 4. Design of the Embedded Electronic Platform

This chapter focuses on the development process of the embedded electronics platform. The design requirements were compiled based on the case study of current approaches and hardware trends of commercial and research prostheses and limitations identified for the *CyberTUM* prosthesis [chapter 2](#). The preliminary results obtained from [chapter 3](#) influenced the design of the hardware required to realise the proposed platform prototype and much of the earlier development work was carried over to the final platform.

Based on the design requirements, suitable components were evaluated and selected and important design decisions are documented. The definitive architecture based on the selected components was then established. The remaining sections delve into hardware design and firmware implementation details of the mechatronic system developed.

## 4.1. Requirements

The high-level requirements for the embedded electronics platform are outlined in Table 4.1. The first column subdivides the entries in two groups: functional and non-functional requirements. The Functional Requirements row presents desired minimum functionality for the prototype. The Non-Functional Requirements row presents requirements oriented towards design flexibility as the platform is intended to cater for future use cases.

Type	#	Requirement	Selection
Functional	1.1	Microcontroller tested in motor control application	Microchip SAMD51 (64pin QFN)
	1.2	Number and type of supported actuators	4 BLDC (trapezoidal)
	1.3	Commutation strategy	Six-step Commutation
	1.4	Cascaded Control of Actuator	Position, Speed and Current Control
	1.5	Support for absolute position feedback on each DOA	Yes
	1.6	sEMG bio-potential signal channels for user control	Yes - up to 8 Channels
	1.7	Support for analog sensors such as FSR sensors for tactile sensing	Yes
	1.8	Support for digital sensors with SPI or I2C interfaces	Yes
	1.9	Support for an IMU to enable Orientation & Gesture Recognition	BNO055(Fixed Firmware) BMF055(Programmable)
	1.10	Real-time capable and deterministic communication interface to enable high level control	EtherCAT
	1.11	Provide necessary power protection to enable portable, battery powered use	eFuse Protection
Non-Functional	2.1	Modular design to allow further expansion or change in functionality	
	2.2	Maintain a single microcontroller vendor to ease development learning curve	
	2.3	Use free tools for Electronics design to enable further development	
	2.4	Electronics platform shall be smaller than hardware in current prototype	
	2.5	Ensure selected components are still in active production	
	2.6	Avoid BGA packages and other difficult to assemble components	

Table 4.1.: Embedded Electronics Platform Requirements Summary

## 4.2. Methodology

The following methodology was adopted during development. Design work started with basic block diagrams, followed by component selection, schematic design, PCB-layout and finally, the generation of a 3D model. All relevant schematics, PCB layouts and design documents are included in [Appendix B](#) for reference and each of the logical system blocks were implemented as design-blocks.

*Autodesk Eagle* was the preferred EDA tool as it was the tool of choice at the [MIRMI](#) institute, which provided an extensive parts library with corresponding component footprints and a large range of components in stock. *Autodesk Fusion 360* was also used extensively as it enabled the linking of the 2D circuit designs to visualise and manipulate designs in 3D, thus allowing for a high-density stacked design to ensure optimal component placement and maintain required clearances, which was invaluable during the design stage. The following strategy was adopted during development:

- Use the design block functionality of *Eagle* to create designs which can be implemented, tested and reused to minimise the routing effort to realise multiples of the same design.
- Use *Atmel/Microchip* drivers and configuration tools where possible to enable visual configuration of peripherals, in this case *ASF4 (Atmel Start)*. Will allow future users to easily customise the firmware to suit new use cases.
- Provide necessary documentation and baseline firmware functionality and drivers to ease continued development of a future prosthetic device based on the platform developed.

## 4.3. Predefinitions & Biases

This section provides an overview of factors which may have swayed design decisions in a particular direction, in addition to those outlined in [section 3.1](#). Due to the limited budget and time available, these considerations were important to make it possible to realise the required hardware and supporting software in time.

- *EtherCAT* and [IMU](#) library provided by [MIRMI](#) were adapted to save development time.
- Global chip shortage meant that many items were not in stock. Designs reflected this by selecting components that were still in stock at [MIRMI](#) because alternatives were not available and had extended lead times.
- *Autodesk Eagle* was used due to the student licence provided and the extensive design block and component library provided by [MIRMI](#) which saved development time.
- A 24 V power source was selected as it is the standard voltage used for designs at [MIRMI](#) and the previous *CyberTUM* prosthesis.
- Mechanical design was outside the scope of this thesis, therefore mechanism selection and packaging restrictions are unknown. The platform was designed to provide as much implementation flexibility in the smallest footprint possible.
- A range of *Faulhaber BLDC* motors were provided by [MIRMI](#) for initial testing and development. The motor control solution was tested and tuned using these motors.

## 4.4. Overall Platform Scope

The diagram in Figure 4.1 presents the overall scope of the platform developed. The items shown in green were designed, implemented and tested. The remaining items were not implemented directly and were either developed by others, are third-party products or are considered future work. The platform presented consists of a functional hardware prototype with corresponding firmware for functions within the dashed envelope.

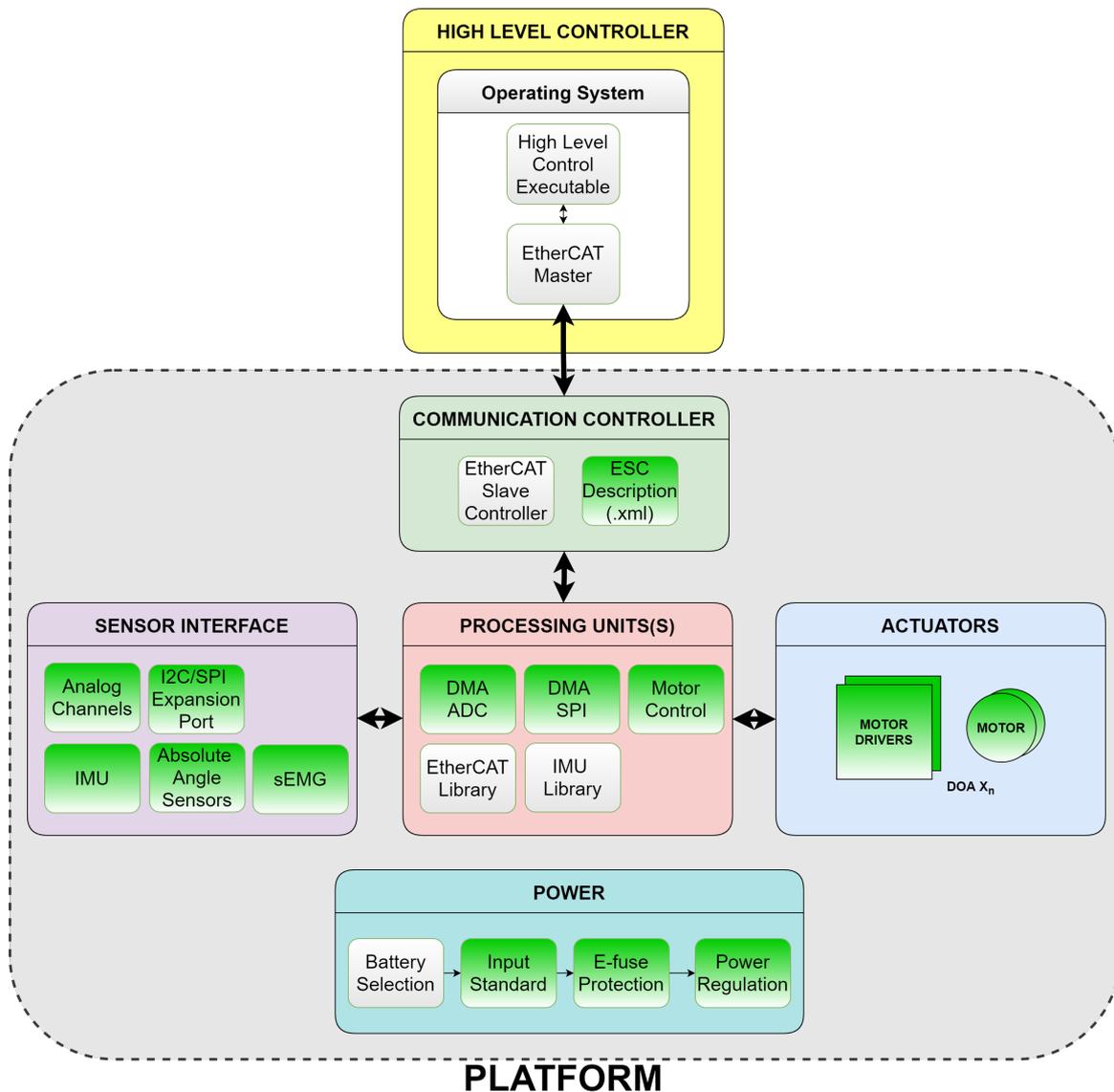


Figure 4.1.: Proposed Platform Architecture

## 4.5. Component Selection

This section presents the components evaluated and selected to realise the various functions outlined in [Figure 4.1](#).

### 4.5.1. Motor Control Hardware

The generalised structure of the [BLDC](#) motor driver was covered in [3.3.1](#) and was carried over. Options for possible alternatives or improvements to the components on the existing motor control hardware provided by [MIRMI](#) were investigated.

#### Motors Provided

The specifications of the [BLDC](#) motors provided by [MIRMI](#) for development and testing are listed in [Table 4.2](#). The control strategy and tuning was tailored to this range of motors. Although, the principle of operation is the same and any [BLDC](#) motor with similar specifications could be used.

Parameters	2214S024BXTR	3216W024BXTR
Supplier	Faulhaber	Faulhaber
Nominal Voltage(v)	24	24
BEMF Type	Trapezoidal	Trapezoidal
Pole Pairs	7	7
Sensors	3 Hall Sensors	3 Hall Sensors
Starting torque(mNm)	29.6	263
Rated torque(mNm)	10.2	40.1
Rated Current(A)	0.37	1.17
Rated Speed (rpm)	2600	4150
Diameter x Length (mm)	22 x 14.8	32 x 16.8
Mass(g)	25.5	57.9

Table 4.2.: Faulhaber BTX series specifications

## Motor Driver IC

Many specialised driver ICs designed to BLDC motors are available on the market. Due to the relatively small size and current requirements of the selected motors, the most economical and space efficient solution was to select a motor driver with integrated power MOSFETs.

The following selection criteria were used to identify suitable components:

- 3 half-bridge drivers with control and timing logic.
- Integrated power MOSFETs.
- 6 PWM or 3 PWM + EN input modes.
- 3.3V interface support.
- Supports for 2A of continuous drive current.
- Compact form factor package with low thermal resistance.
- Built in protection features such as Over Current Protection (OCP), Under-Voltage Lock Out (UVLO) and Over Temperature Protection (OTP).

Based on the selection criteria, a shortlist was prepared shown in Table 4.3.

Parameters	DRV8313	DRV8316	MP6540H
Supplier	TI	TI	MPS
Voltage Range(V)	8-60	4.5-35	5.5-50
Max Output current (A)	2.5	8	5
Max Sw Frequency(kHz)	250	200	196
On Res HS/LS (mOhm)	78	100	45
Control Mode	6/3xPWM	6/3xPWM	6/3xPWM
Package	QFN-36	QFN-40	QFN-26
Size (w x h)	6mm x 6mm	7mm x 5mm	5.1mm x 5.1mm
Protection Features	OCP,UVLO,OTP	OCP,UVLO,OTP	OCP,UVLO,OTP
Integrate CS Amplifier	No	Yes	Yes
MIRMI In-Stock	Yes	No	No
Active part	Yes	Pre-Prod Samples	Yes
Available (during design)	Yes	Samples Only	No

Table 4.3.: Motor Driver Shortlist

The *MP6540H* would have been the preferred choice as it supports a higher output currents in a compact form factor; however, due to the current global shortages experienced, the design proceeded with the tried and tested *DRV8313* which has been used previously and was in stock at *MIRMI*.

## Current Sensing

Accurate measurement of phase currents of a BLDC motor is essential for closed loop current control, but it is also important to limit the motor current in the case of an overload or stall

condition to prevent damage to the motor or the driver stage. Several common approaches are used to measure motor phase current including inline, high-side and low-side sensing respectively shown in Figure 4.2.

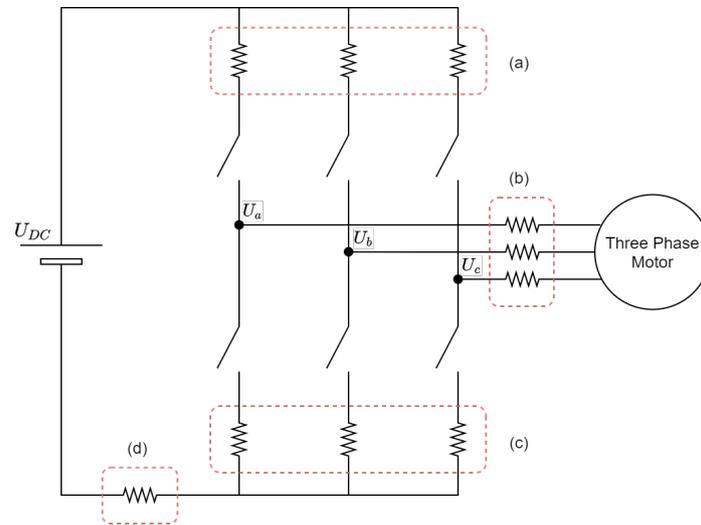


Figure 4.2.: (a) High-side (b) Low-side (c) Inline (d) DC bus current sensing topology

The most common approach is low-side sensing, and many motor drivers such as the *DRV8316* and *MP6540H* listed in Table 4.3 have integrated current sense amplifiers for phase current measurement with shunt resistors. This is preferable to the equivalent high-side sensing approach as it does not require amplifiers that support high voltages found at the high side. The main drawback of both high- and low-side sensing is the strict ADC sampling synchronisation requirement to the respective switching event while the MOSFET is conducting the relevant phase current. A similar arrangement with single current shunt connected across all three phases is also possible, but timing requirements and the three phase current reconstruction is even more complex.

The inline sensing method is the simplest and provides a true indication of the phase current, regardless of the PWM duty cycle. A summary of the pros and cons of each approach are provided in Figure 4.3. Inline sensing was selected due to the true phase current measurement possibilities.

High-Side Implementation	Low-Side Implementation	Inline Implementation
<b>Pros</b>		
Stable high common-mode voltage	Low common-mode voltage	
Fault detection	Low voltage amplifiers acceptable	Know the true phase current
Robust amp requirements	Low cost	Gain the ability to monitor the system
No ground disturbances		
<b>Cons</b>		
Drive current $\neq$ phase current	Unable to detect faults	Sense amp must support high common-mode rejection
	Drive current $\neq$ phase current	

Figure 4.3.: Summary of Current Senses Topologies [Jas10]

For inline sensing, the traditional shunt resistor and amplifier approach requires resistors with tight tolerances and high handling capabilities. Furthermore, resistors introduce power loss and voltage drops into the power path. For these reasons, specialised Hall effect current sensor ICs are considered superior in this application.

The current sensors had to meet several criteria to qualify for the design:

- Bi-directional current measurement.
- Suitable measurement range less than 10A and high sensitivity to high current measurement resolution.
- High bandwidth for fast control cycles and low full scale error over a wide temperature range.
- Small form factor for compact layout.

Parameters	ACS70331-2P5B3	CQ330G	ACS711KL
<b>Supplier</b>	Allegro	AKM	Allegro
<b>Supply Voltage</b>	3-4.5	4.5-5.5	3.3-5
<b>Current Range(A)</b>	±2.5	±4.5	±10
<b>Bandwidth(kHz)</b>	1000	1000	100
<b>Sensitivity (mv/A)</b>	400	450	110
<b>Total Output Error (%FS)</b>	±2.4	±2.2	±5
<b>Package</b>	QFN-12	VSOP-24	SOIC-8
<b>Size (w x h)</b>	3mm x 3mm	7mm x 5mm	4.9mm x 6mm
<b>MIRMI In-Stock</b>	Yes	No	No
<b>Available(Des. Time)</b>	Yes	Samples Only	No

Table 4.4.: Current Sensor Shortlist

Given the selection criteria, a shortlist was prepared, as shown in [Table 4.4](#). The *ACS70331* series was selected due to the high bandwidth, sensitivity and small form factor compared to the other solutions available. Due to the current global shortages experienced, the other Hall based current sensors with comparable bandwidth and sensitivity, such as the *CQ330G*, were not available.

### 4.5.2. Joint Position Sensing

Based on the the requirements outlined in [section 4.1](#), a solution for obtaining the absolute position of each [DOA](#) was required. Numerous absolute position measurement solutions are available, but non-contact, Hall sensor based solutions for measuring the rotation of a permanent magnet are the most flexible. Some of these are also suitable for both on-axis and off-axis applications, as shown in [Figure 4.4](#), which increases design flexibility as the sensor does not need to be directly attached to the axis center line. These solutions are usually more reliable and economical than similar restive or transformer based solutions.

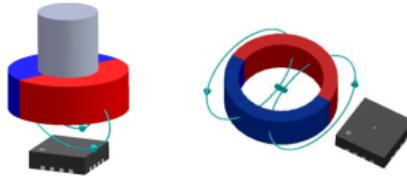


Figure 4.4.: On vs Off Axis sensing [[Mon10](#)]

Strategic placement of this kind of sensor and magnet arrangement would allow the position of a gripper, finger or wrist, for example, to be determined even after power is lost as the permanent magnets orientation can always be determined in an absolute manner. Using other methods such as the motor integrated Hall sensors is also possible, but this solution is relatively low resolution and the position reference is lost when power is interrupted. Several promising devices were shortlisted. See [Table 4.5](#).

Parameters	AS5048A-HTSP	A1335LLETR	MA730GQ-P
Supplier	AMS	Allegro	MPS
Resolution(bits)	14	12	12
Interface	SPI,PWM <sup>1</sup>	SPI,I2C,SENT	SPI,UVW,PWM
SPI/I2C Freq(MHz)	10/3.4	10/0.4	25/N/A
Max Sample Rate (Khz)	11	32	1000
Max RPM	N/A <sup>2</sup>	N/A <sup>2</sup>	60,000
Daisy Chain Support	Yes	N/A <sup>2</sup>	N/A <sup>2</sup>
Off-axis Measurement	No	Yes	Yes
Supply Voltage(V)	3.3-5	4.5-5	3.3-5
Package	TSSOP-14	TSSOP-14	QFN-16
MIRMI In-Stock	Yes	No	No
Available (Des. Time)	Yes	Yes	No

<sup>1</sup> I2C version available

<sup>2</sup> Not specified in datasheet

Table 4.5.: Absolute Angle Sensing Shortlist

The *A1335* and *AS5048* were selected for evaluation as they support both [SPI](#) and [I2C](#) interfaces which provides implementation flexibility, allowing sensors to be daisy-chained. The off-axis sensing capabilities of the *A1335* were also of interest to improve sensor integration flexibility. These sensors were also selected based on availability.

### 4.5.3. EtherCAT Communication

*EtherCAT* was preselected as the communication protocol of choice. In order to communicate with *EtherCAT*, a suitable [EtherCAT Slave Controller \(ESC\)](#) is required and a survey of available [ESC](#) was performed. As mentioned in [section 4.1](#), the use of [BGA](#) packages is avoided for prototyping and this limits the available options. Promising candidates are listed in [Table 4.6](#).

Parameters	LAN9252	LAN9253	AX58100
<b>Supplier</b>	Microchip	Microchip	ASIX/ST
<b>Supply Voltage(V)</b>	3.0-3.6	3.0-3.6	3-3.6
<b>Fieldbus MMUs</b>	3	8	8
<b>SyncManagers</b>	4	8	8
<b>Distibuted Clock Support</b>	Yes	Yes	Yes
<b>DPRAM(Kb)</b>	4	8	8
<b>Communication</b>	SPI/QSPI	SPI/QSPI	SPI
<b>Max SPI Frequency(MHZ)</b>	30/80	30/80	50
<b>Package</b>	TQFP&QFN-64	QFN-64	QFP-80
<b>Available (design time)</b>	No	No	No
<b>MIRMI In-Stock</b>	Yes	No	No
<b>Lead Time</b>	1/3/2022	11/6/2022	N/A

Table 4.6.: EtherCat Slave Controller Solutions

The *LAN9252* was selected due to availability and [MIRMI](#) software library support. The *LAN9253* would have been preferable as it is the successor to the *LAN9252* and includes several improvements, such as a simpler communication interface, unfortunately neither of the alternative solutions in [Table 4.6](#) were available at design time due to global shortages and the design and prototypes had to rely on local stock at the institute.

#### 4.5.4. Inertial Measurement Unit (IMU)

IMUs that integrate a number of motion sensors into one device and can provide high accuracy positioning information are now commonly found in a vast amount of devices. IMUs are able to measure 6-DOF or 9-DOF and typically feature 3 axis gyroscopes, accelerometers and magnetometer sensors. Motion tracking using IMUs employs sensor fusion to derive a single, high accuracy estimate of the device orientation. Sensor fusion software combines the IMU's various motion sensor outputs using complex mathematical algorithms. This is computationally expensive and would require valuable host controller resources to continuously process the sensor data stream.

Recent advances in sensor technologies have integrated a dedicated processing core to offload the sensor fusion task from the host processor which is desirable in this application as it does not compete for resources with tasks such as motor control. A summary of devices investigated which support integrated sensor fusion are shown in Table 4.7.

Parameters	BNO055	BMF055	BNO080
Supplier	Bosch	Bosch	HillChrestLabs
Supply Voltage(V)	2.4-3.6	2.4-3.6	2.4-3.6
Digital Interface	I2C&UART	I2C&UART	I2C&UART
DOF	9	9	9
Integrated Sensor Fusion	Yes	Yes	Yes
User Programmable	No	Yes	No
Max I2C Frequency(kHz)	400	400	400
Max Fusion Update Rate(Hz)	200	App dependent	400
Interrupt Support	Yes	Yes	Yes
Package	LGA-28	LGA-28	LGA-28
Size (w x h)	3.8mm x 5.2mm	3.8mm x 5.2	3.8mm x 5.2
MIRMI In-Stock	Yes	Yes	No
Available (design time)	No	No	No

Table 4.7.: IMU Solutions with integrated Sensor Fusion

The design proceeded with the *BMF055* due to the integrated user programmable processor core which caters to future use cases in prosthesis control techniques and evaluation of different sensor fusion algorithms. All the sensors are actually pin compatible as they are based on the same underlying hardware, only differing in the bundled fusion software implementation. Unfortunately, none of the devices listed in Table 4.7 were available at design time due to global shortages and the prototypes production had to rely on local stock at the institute.

### 4.5.5. sEMG Acquisition system

Based on limitations experienced with the the *MyoWare* series sensors and the signal characteristics discussed in [chapter 2](#), it was clear that a new low noise, high gain and high resolution [Analog front end \(AFE\)](#) was required for reliable signal acquisition from the [sEMG](#) electrodes. The design of a precision [AFE](#) and data acquisition system is not a trivial task, two options were considered which focused on either adapting a proven open source design or using commercially available [Application-specific integrated circuit \(ASIC\)](#) designs intended for bio-potential signal acquisition.

#### Discrete & ASIC Solutions

Initial efforts were based on creating a multi-channel version of existing open source designs, such as the the *Bitario* [[BIT11](#)], which implement the required filtering, amplification and rectification using discrete op-amps and instrumentation amplifiers to produce a signal which can then be sampled by a microcontroller. Once scaled up to eight channels, it became clear that this system would quickly become complex to implement, tune and test and require significant board space.

Several commercial solutions exist that are specifically targeted towards multi-channel bio-potential signal acquisition. Notable examples include the *ADS129x* series from *Texas Instruments* and *RHA2216* from *Intan*. These fully integrated solutions contain an [Analog front end \(AFE\)](#) which performs the required filtering, amplification and sampling with high resolution [ADC\(s\)](#) to digitise the bio-potential level signals and present the results over a standard [SPI](#) interface. This approach was selected as it greatly simplifies the design and saves valuable board space and microcontroller resources.

#### Analog Front End (AFE) Requirements

An [AFE](#) is used to acquire and transform the analogue [sEMG](#) signal to a digital representation for further transfer through the system. The [AFEs](#) that exist on today's market come mainly in two forms, those with [ADCs](#) installed and those without. Below are different [AFE](#) characteristics of importance.

Characteristic	Description
<b>Samples Per Second (SPS)</b>	As shown in <a href="#">section 2.2</a> , the frequency characteristics of <a href="#">sEMG</a> signals dictate that a sampling rate of around 1000 is required due to the <i>Nyquist-Shannon Sampling Theorem</i> , signals should also be low-pass filtered before sampling to avoid aliasing.
<b>ADC Resolution</b>	Common resolutions available include 16 and 24 bits. The benefit of 24 bit is the dynamic range which allows enhanced signal discrimination of noise and the <a href="#">EMG</a> signal.
<b>Amplification (Gain)</b>	The low signal amplitude obtained by <a href="#">sEMG</a> require amplification to produce workable results. Low gain can, to some extent, be compensated for by dynamic range afforded by a 24 bit resolution.
<b>Common mode rejection rate (CMRR)</b>	A high <a href="#">CMRR</a> is desirable as it rejects noise common to both of the differential inputs. Ideally, only the difference between the two input lines is amplified while ignoring any common-mode noise. The source of a common-mode noise is typically nearby AC mains frequencies (50Hz or 60Hz).
<b>Input referred noise (IRN)</b>	Both the <a href="#">AFE</a> and the internal <a href="#">ADC</a> are prone to a certain amount of input noise. The lower IRN, the better for the signal fidelity which is an important differentiating factor.

Table 4.8.: EMG AFE Requirements

A summary of the relevant specification of devices investigated is listed in [Table 4.9](#).

Parameters	ADS1299	ADS1298	RHD2216
<b>Supplier</b>	TI	TI	INTAN
<b>ADC Resolution(<i>bits</i>)</b>	24	24	16
<b>ADC Architecture</b>	Delta-Sigma	Delta-Sigma	SAR
<b>Channels</b>	4,6,8	8	16
<b>Input-referred Noise (<math>\mu V_{rms}</math>)</b>	0.1	2.4	2.4
<b>Gain(<math>V/V</math>)</b>	1,2,4,6,8,12	1,2,4,6,8,12,24	200
<b>Max Sampling Rate (<i>ksps</i>)</b>	16	32	30
<b>Interface</b>	SPI	SPI	SPI
<b>Digital Voltage(<math>V</math>)</b>	1.8 - 3.3	1.8 - 3.3	1.8 - 3.3
<b>Analog Voltage(<math>V</math>)</b>	4.74-5	2.7- 5.25	3.2-3.6
<b>Integrated ADC</b>	Yes (8)	Yes (8)	Yes (1)
<b>CMRR(<math>dB</math>)</b>	-120	-84	100
<b>Package</b>	TQFP-64	TQFP-64	QFN-56
<b>Approx Price (<i>Euro</i>)</b>	60	54	180
<b>MIRMI In-Stock</b>	No	No	No
<b>Available (Des. Time)</b>	Yes	No	No <sup>2</sup>

<sup>1</sup> Multiple versions available

<sup>2</sup> Only available directly from manufacturer

Table 4.9.: EMG AFE Shortlist

The *ADS1299* was selected based availability and the level of integration offered at relatively

low cost compared to the *RHD2216*. The *ADS129x* series is popular in both industry and the research community. Several open source designs such as *OpenBCI* exist featuring the *ADS1299* and have been successfully used for , [EMG](#) and applications. The excellent TI and open source community documentation and reference designs also provided valuable design guidance. The *ADS1299* was benchmarked by [\[Ras+18\]](#) and [\[MOCH52\]](#) and shown to be comparable to laboratory based systems and competitors based on the *RHD2216*.

### ADS1299 Additional Components

For best performance, TI recommends operating the *ADS1299* with a 3.3V supply voltage for the digital section and bipolar  $\pm 2.5V$  supply voltages for the analogue section. A dedicated *RP115H* 3.3V regulator was selected for the digital section and the +2.5 is obtained from using *TLV700* regulator. The  $-2.5V$  is provided by first inverting the digital section 3.3V using a *MAX1697U* charge pump inverter feeding a *TPS723* negative output regulator.

The *ADS1299* datasheet also recommends additional low pass filtering to supplement the digital filtering performed inside the device. A simple RC filter is provided to attenuate frequencies and their harmonics above about 1MHz which are not covered by the internal filters. Input protection is also recommend to protect the sensitive input stage from [Electrostatic discharge \(ESD\)](#) and the *TPD4E1B06DC* is specifically provided for this. Each of the input signals connected to the *ADS1299* passes through the circuit arrangement shown in [Figure 4.5](#) which performs the required transient voltage suppression and low pass filtering.

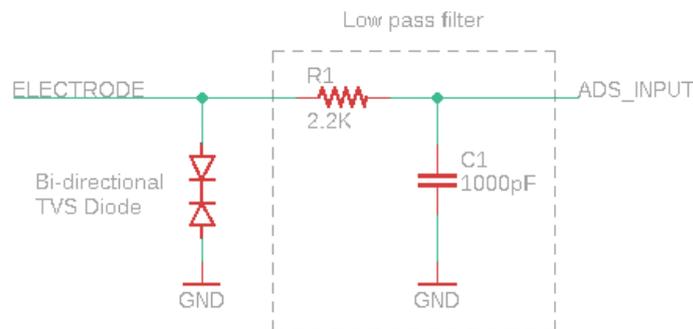


Figure 4.5.: Input Filtering

### sEMG Electrodes

Suitable electrodes need to be attached to the skin in precise locations to target certain muscle groups. In this preliminary implementation, a harness for four channels of detection plus one reference channel is provided as shown in [Figure 4.6](#). The red and blue electrodes form the differential pair used to measure each target muscle's activity, while the black electrode acts as a reference and is usually placed where no muscle activity is expected. The harness was created by modifying several *CAB-12970* sensor cables and terminating them to a 20-Pin *Molex Milli-Grid* 2.00 mm-Pitch Female Connector.

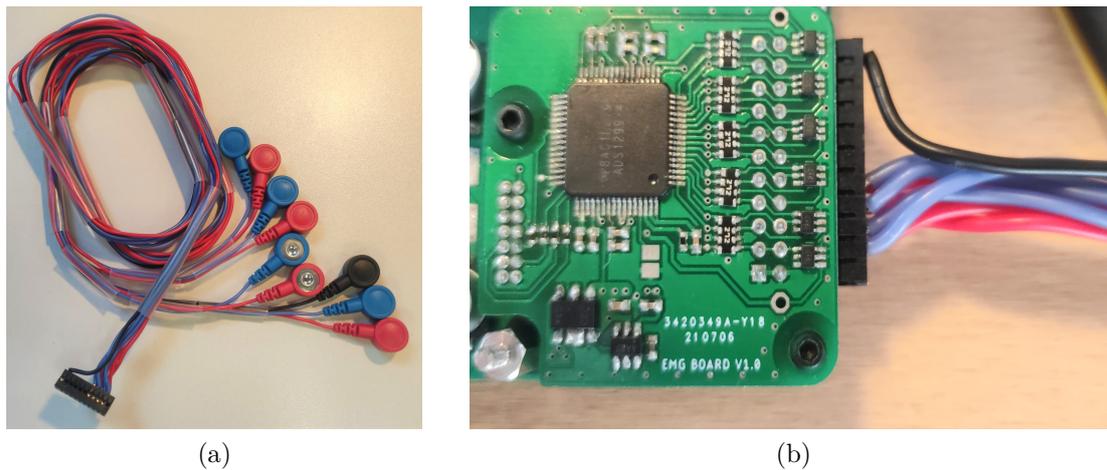


Figure 4.6.: (a) Four Channel sEMG harness (b) Harness connected to Input header

#### 4.5.6. Force-Sensing Resistor (FSR)

In order to provide the hardware required to effectively use ubiquitous [Force-Sensing Resistor \(FSR\)](#) type sensors commonly used for tactile force measurements, it is necessary to understand the characteristics of the sensors. [FSRs](#) exhibit an approximately exponential decrease in resistance with an increase in the force applied, whereas the conductance increases linearly with force as shown in [Figure 4.7](#).

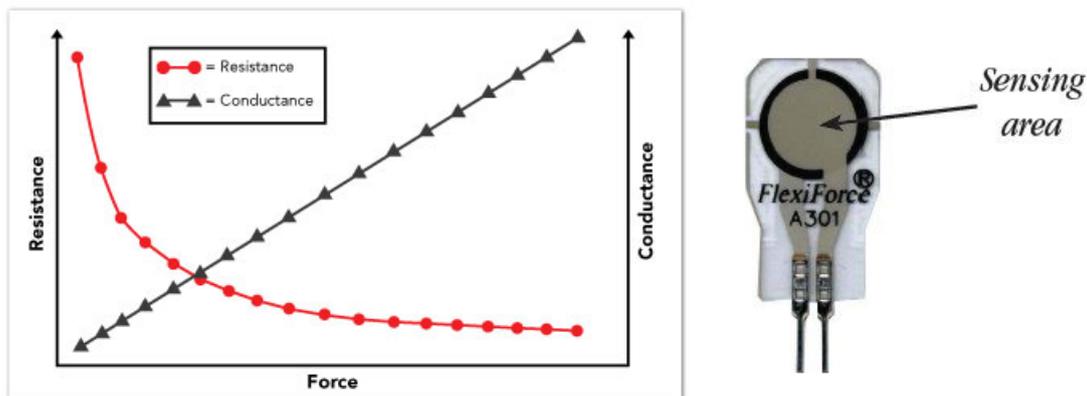


Figure 4.7.: FSR sensor Response [[Tek21](#)]

#### Signal Conditioning

Several approaches are commonly used to provide the required signal conditioning to interface with these sensors, including a simple voltage divider, an op-amp buffered voltage divider or a transimpedance amplifier configuration. Exploiting the linear conductance relationship in favour of simpler voltage divider arrangements produces a more linear force response and better utilises the conversion range of an [ADC](#) as shown in [Figure 4.8](#),

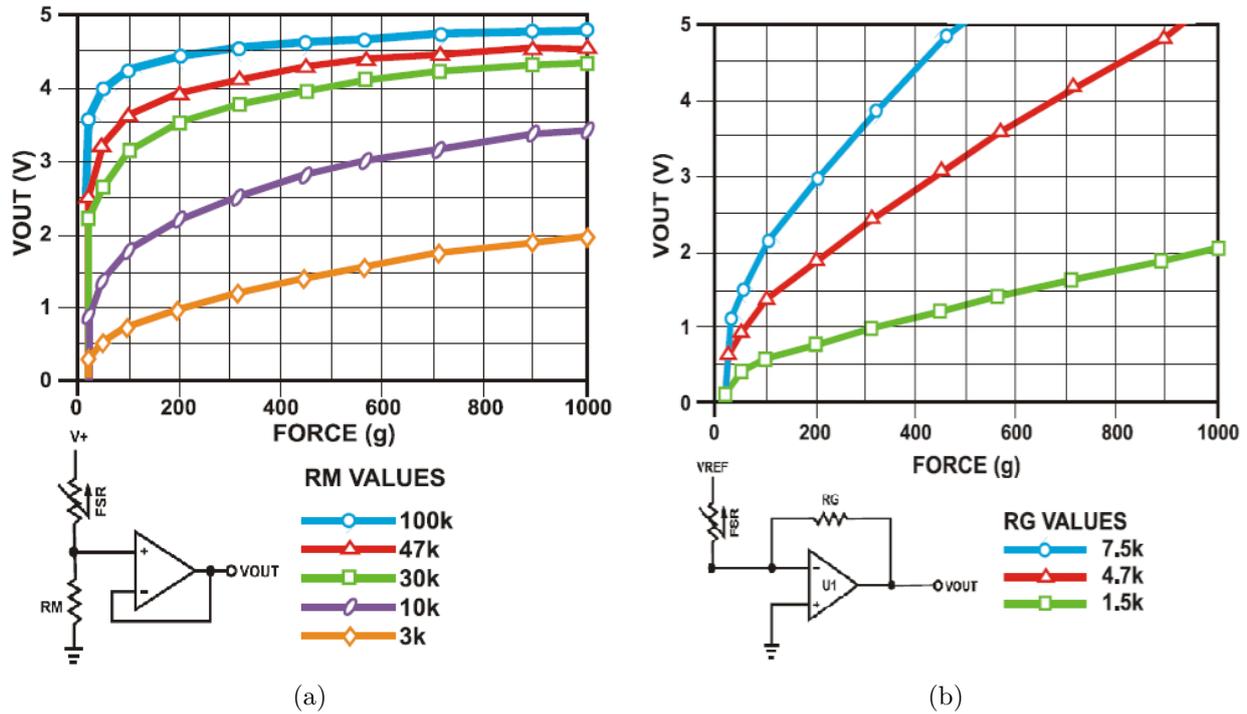


Figure 4.8.: (a) Voltage Divider (b) Trans-impedance amplifier [Int]

The required signal conditioning circuit is based on a transimpedance amplifier shown above. The output of the amplifier is described by the following equation:

$$V_{out} = V_{ref} \left[ \frac{-R_G}{R_{FSR}} \right] \quad (\text{Eq. 4.5.1})$$

From this, it is evident that a negative reference is necessary to yield a positive output. Value of  $R_G$  determines the output slope.

### Op-amp Selection

The selected transimpedance amplifier based design requires a suitable op-amp. The following selection criteria were used to identify suitable components based on the recommendations outlined in [Int]:

- Low input bias current (in the range of nA or pA).
- JFET or CMOS inputs.
- Bandwidth / slew rate compatible with sample rate requirements.
- Rail-to-rail operation to maximise output range.
- Quad op-amp package to maximise space efficiency.

A summary of the relevant specification of suitable rail-to-rail op-amps reviewed is listed in [Table 4.10](#). The *AD806R* was selected due to the combination of low offset and bias current and wide operating voltage range.

Parameters	LMV324	OPA1644	AD8609R
Supplier	TI	TI	AD
Operating Voltage(V)	2.7-5	$\pm 2.25$ to $\pm 18$	1.5-5
Input Type	CMOS	JFET	CMOS
Opamp Count	4	4	4
Input Offset( $\mu$ V)	76	66	50
Input Bias Current(pA)	11	2	1
Package	SOIC-14	SOIC-14	SOIC-14
MIRMI In-Stock	No	No	No
Available (Des. Time)	Yes	Yes	Yes

Table 4.10.: Quad Op-amp Specification Summary

### FSR Additional Components

The additional components selected to implement the transimpedance amplifier arrangement included a *MAX6070* 3V voltage reference and *MAX1697* inverting charge pump used to provide the -3V used to bias the [FSR](#) sensor and ensure a positive op-amp output. The same input protection circuit as [4.5.5](#) was also included on the [FSR](#) inputs to protect the system from [ESD](#) and provide low pass filtering

### 4.5.7. Power Supply & Protection

The portable nature of a prosthesis requires the use of a battery to power the device. Lithium cells of various chemistries have become the predominant energy storage means used by myoelectric prostheses due to the higher energy density compared to technologies such as [NiCd](#) and [NiMH](#). Li-ion systems must be correctly designed to achieve good performance and avoid serious safety hazards that can result from battery cell abuse and improper operation. Overcharging, over discharging, overheating, short-circuiting or damaging a charged Li-ion battery can result in fire or explosion [[Lig](#)]. While many modern, commercially available battery packs provide integrated battery management and protection features, the decision was made to integrate an additional e-Fuse to ensure safe operation of the system while powered from any power source.

An eFuse, or electronic fuse, can replace conventional fuses and offers faster and more accurate intervention, without requiring replacement after actuation. In addition to [Over Current Protection \(OCP\)](#), an eFuse allows for protection against over voltage, under voltage, short circuit, inrush current limitation and reverse polarity events. The [Under-Voltage Lock Out \(UVLO\)](#) threshold can be set to prevent over-discharging the battery.

A variety of integrated solutions exist and a shortlist of suitable solutions is shown in [Table 4.11](#).

The *TPS26636* was selected as it offers the the most flexibility, with the fewest external components required, in the smallest physical package due to the integrated [MOSFET](#). The parameters

Parameters	LT4356	STEF01FTR	TPS26636
Supplier	AD	ST	TI
Voltage Range(V)	4-80	8-48	4.5-60
Continuous current (A)	N/A <sup>1</sup>	4	6
Current Limit(A)	Adjustable	3.2-4.8A	0.6-6A
Inrush Limit	Yes-Adjustable	Yes-Adjustable	Yes-Adjustable
Protection Features	OCP,UVLO,OTP	OCP,UVLO,OTP	OCP,UVLO,OTP
Integrated MOSFET	No	Yes	Yes
Integrated Cur Sense Res	No	Yes	Yes
Reverse Polarity Protection	Yes <sup>2</sup>	Yes <sup>2</sup>	Yes <sup>2</sup>
Package	MSOP-10	HTSSOP-14	HTSSOP-20
Size (w x h)	4mm x 3mm	6.4mm x 4mm	4mm x 4mm

<sup>1</sup> External MOSFETs limited

<sup>2</sup> With External MOSFETs

Table 4.11.: eFuse IC Shortlist

used to configure the *TPS26636* are provided in [Appendix C](#). Additionally, a self-contained *TRN-3-2411SM* switch mode regulator was selected for the 5V rail as it includes a wide 18-36V operating range and the 600mA output in a compact form factor. The *RP115H* regulator was selected as the default for the 3.3V duties and both components are frequently used and readily available at [MIRMI](#).

#### 4.5.8. Additional Components

Connector selection is important to ensure reliable connections between boards and external components. Connectors usually determine design parameters such as stack heights and minimum board dimensions. Finding appropriate motor connectors was challenging as compact, low profile and secure connectors with high current handling proved difficult to find. The *Molex Pico-Lock* series of connectors was one of few which fulfilled the requirements, allowing for a lower stack height while still being rated for up to 6A of current. This range of header, mating connectors and crimping tools were then provided by [MIRMI](#). The connector standards established are summarised in [Table 4.12](#):

Interface	Supplier	Part Number	Description
SPI & I2C Sensors	MOLEX	503763-0691	Pico-Lock 1.0 for all Sensors
Hall Sensors	MOLEX	503763-0591	Pico-Lock 1.0 for hall Sensors
Motor Phases	MOLEX	205338-0003	Pico-Lock 2.0 for Motor Connection
Master Expansion	SAMTEC	CPL-107-02-G-D	Used for EMG Expansion Board
Slave Expansion	SAMTEC	CPL-110-02-F-DH	Used for Analog Expansion Board

Table 4.12.: Header Standard Selection

The same pin configuration was used for all digital sensors and 5V power and data lines share the same connector. The connected sensors need to implement the required daisy-chain routing configuration.

## 4.6. Definitive Architecture

The final development step was the design of a functional hardware prototype to implement all the design requirements set forth in [section 4.1](#) using the components selected in the previous section. The development process involved [Printed Circuit Board \(PCB\)](#) design which integrated existing design blocks and incorporated new features. The prototypes were then fabricated, assembled and tested. Firmware was developed to implement the required functionality and verify the function of the core components of the system. The provided software implementation, CAD designs and documentation act as a reference for users who intend to use the electronics platform in the future.

Based on the computational resource analysis in [section 3.4.5](#) and microcontroller [GPIO](#) and peripheral analysis, it became clear that a minimum of two microcontrollers would be required to implement all the required functionality. The result was a master/slave controller arrangement where the platform functionality is distributed between the two controllers to maximise resource utilisation and allow for a space efficient design. The high level architecture of the prototype is presented in [Figure 4.9](#) and a detailed summary of microcontroller pin allocation is provided in [Appendix A](#).

### 4.6.1. Full Architecture Overview

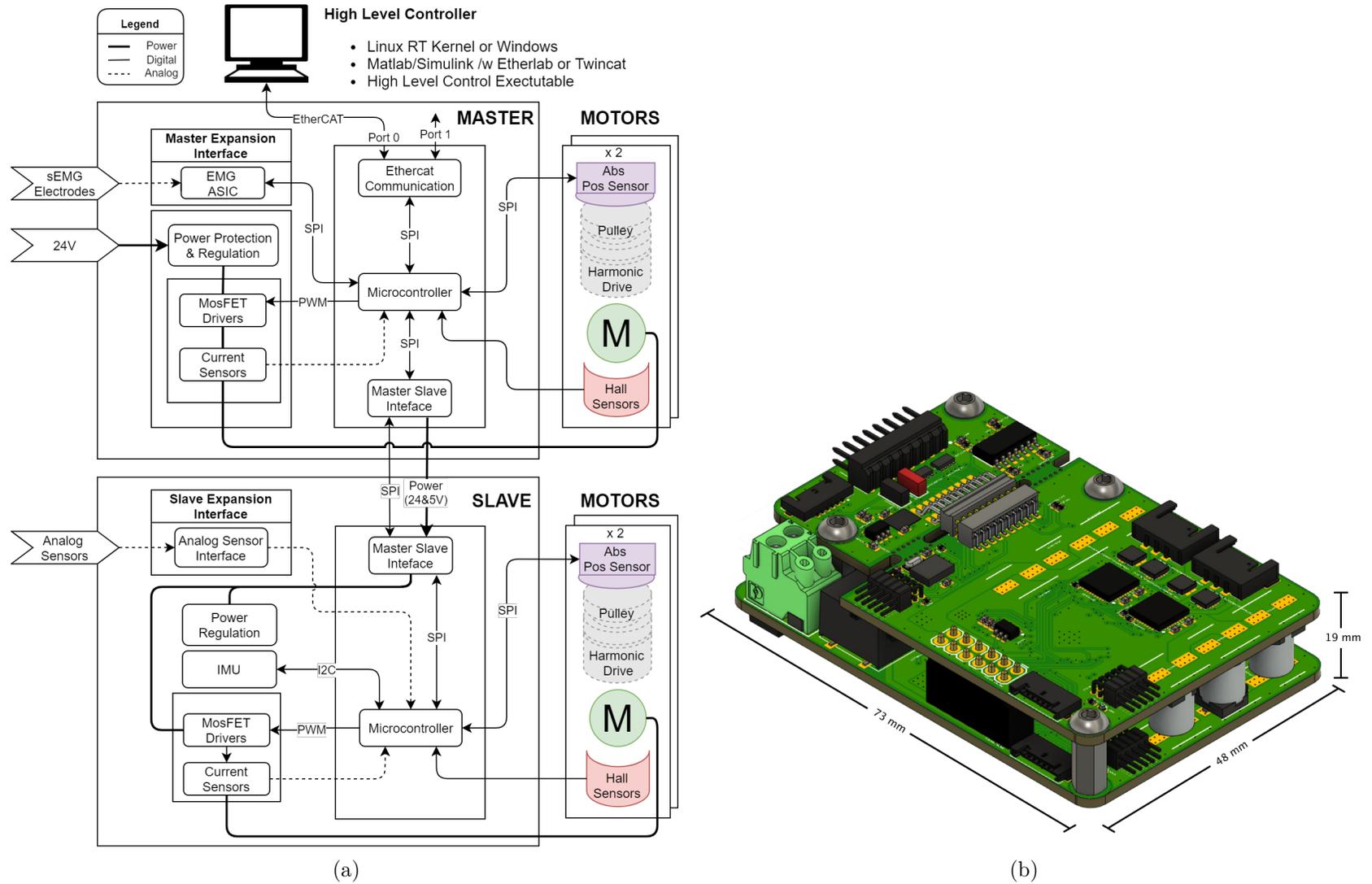
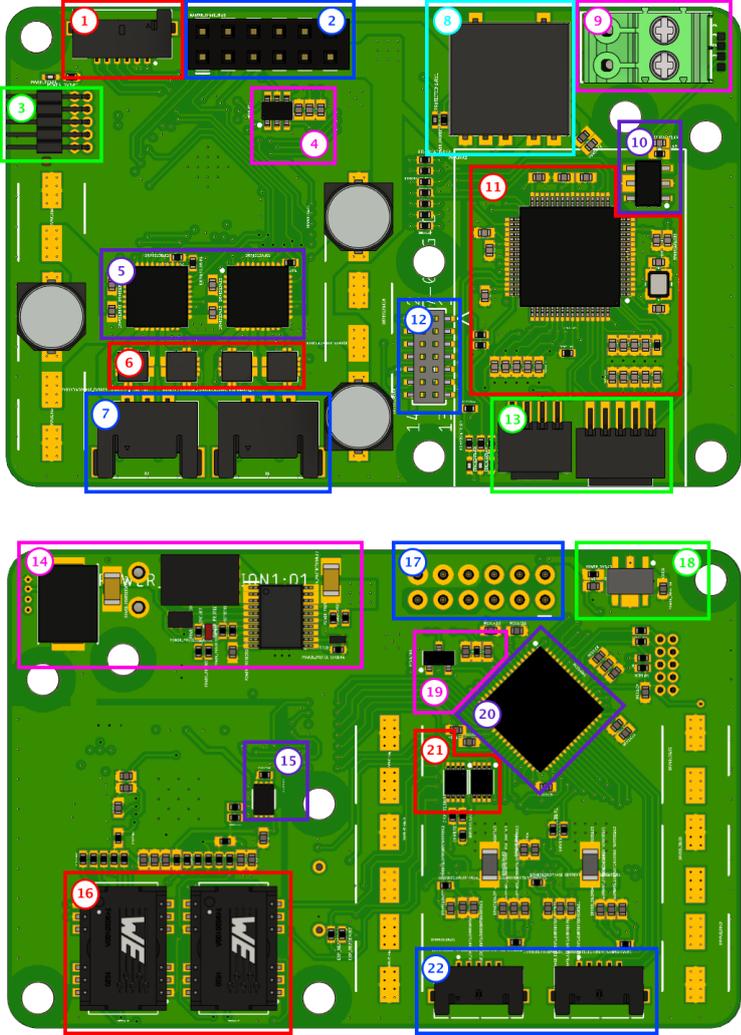


Figure 4.9.: (a) Full Architecture Overview (b) Fully assembled 3D view of PCB stack

### 4.6.2. Master Control Board (MCB)

The **MCB** is based on a four layer design and is responsible for several important functions. The microcontroller acts as the **SPI** master for a number of connected peripherals. First, is the **EtherCAT Slave Controller (ESC)** which enables *EtherCAT* communication with a high level controller. Second, is the **EMG ASIC** used to obtain readings from the **sEMG** electrodes. Finally, the master/slave interface enables power sharing and synchronous board to board communication to transfer the *EtherCAT* data from both boards to and from the high level controller. The board also implements the required power protection and regulation features to allow for safe, tethered and battery powered operation. The motor control and the absolute position sensors duties are duplicated between the the **MCB** and the **Slave Control Board (SCB)** to provide synchronous control over the four **DOA** provided. Important design features are summarised below and the complete design documents are provided in **Appendix B**.

An overview of the master controller board is shown in **Table 4.13**.



No.	Description
1	Angle Sensor Connector
2	Master Slave Interface
3	Programming Header
4	3.0V Voltage Reference
5	Motor Driver ICs
6	Current Sensors
7	BLDC Motor Connector
8	24V to 5V Regulator
9	24V Input Connector
10	EtherCAT 3.3V regulator
11	EtherCAT LAN9252 ASIC
12	Master Expansion Interface
13	EtherCAT In & Out
14	E-Fuse Power Protection
15	LAN9252 ASIC EEPROM
16	EtherCAT LAN Transformers
17	Master Slave Interface
18	Main 3.3V Regulator
19	Reference Divider
20	SAMD51 Microcontroller
21	Motor Drive Latch IC
22	Motor Hall Sensor Connector

Table 4.13.: Top and Bottom Overview of Master Control Board

The relevant dimensional information and stacking arrangement with the [EMG](#) expansion board are shown in [Figure 4.10](#).

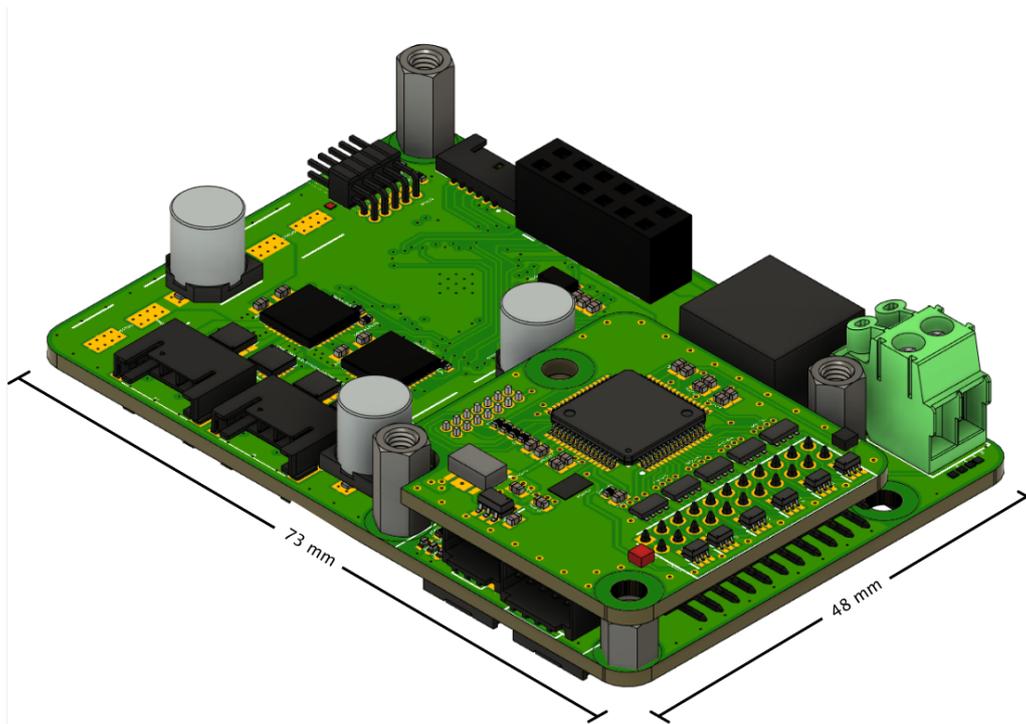


Figure 4.10.: Master control board with attached EMG expansion board

## Microcontroller

The 64-Pin QFN package of microcontroller was pre-selected and is the smallest package available with the required functionality. All pins are fully utilised, and the complete [GPIO](#) allocation list is provided in [Appendix A](#).

The required microcontroller supporting components and routing guideline were based on the *Xplained Pro* board reference implementation [[Mic11](#)]. A summary of the other important design features are provided in the list below:

- In order to save board space and [GPIO](#) pins, the internal oscillator was used to generate the the 100MHz clock frequency.
- The voltage regulator integrated into the microcontroller is used to provide the 1.2V required by the processor core from a single 3.3V rail.
- To maximise the accuracy of analogue measurements, a precision low noise, low drift *MAX6070* 3.0V reference was used.
- [ADC1](#) is configured in differential mode to maximise the dynamic range available. A precision resistor network provides the required 1.5V common mode voltage. This arrangement was chosen to match the common mode voltage to the 1.5V offset voltage of the bi-directional current sensor which corresponds to zero current flow.

## Power Protection & Regulation

The master control board provides the required components to regulate the nominal 24 V input voltage to stable 5 V and 3.3 V rails. An eFuse circuit provides the required protection features and full design parameters were calculated and summarised in [Appendix C](#)

## Position Sensor Interface

The position sensor interface uses the standardised sensor connector used for SPI and I2C based sensors. The interface is intended to be used in the daisy-chain configuration shown in [Figure 4.11](#). The daisy-chain configuration allows for an arbitrary number of sensors which support the daisy-chain to be connected with just four data lines. The connected sensors need to implement the required daisy-chain signal routing configuration.

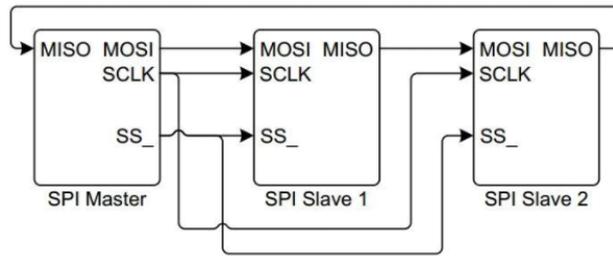


Figure 4.11.: SPI Daisy Chain

## Expansion Interface

The expansion interface was designed to allow new expansion board concepts to be developed without needing to modify the MCB. Currently, the interface is used to implement the required EMG functionality. The connector pin configuration and dimensional information when developing future expansion boards is provided in [Appendix D](#).

A summary of the important implementation features are provided below:

- The interface supports both SPI and I2C connections. The footprints for the required pull-up resistors for the I2C data lines are provided but not populated.
- The interface supplies 5 V power to maximise compatibility as well as two GPIO pins which can be used for analogue inputs, digital inputs/outputs or for external interrupts.
- The connector and mounting hole locations have been defined to allow for secure mounting of the expansion PCB with M2.5 or M3 standoff fasteners.

## Master Slave Interface

The master/slave interface is responsible for both power and data communication between the master control board and slave control board. The pin configuration is shown in [Figure 4.12](#)

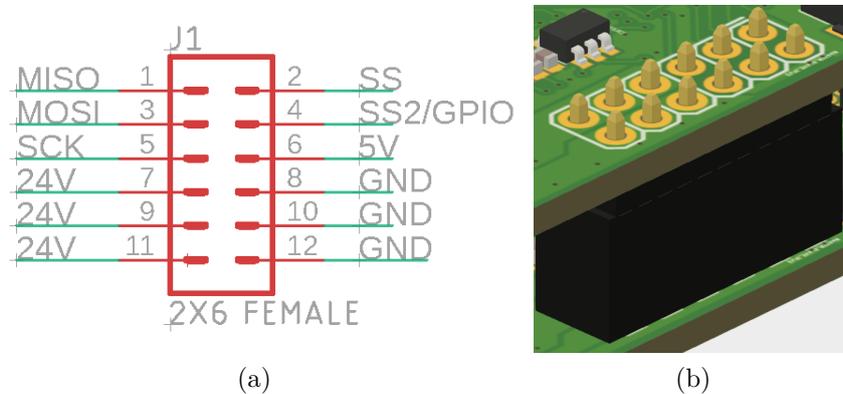


Figure 4.12.: (a) Master Slave Interface pin-out (b) Mated Header

A summary of the important implementation features are provided below:

- The [SPI](#), 5V, 24V and ground signals share the same female connector to create a secure board to board connection when combined with the male header on the slave control board.
- There is a provision for a second slave select (SS) pin which could be used to add an additional [SCB](#) in the future for up to six [DOA](#), but this configuration was not tested.
- A standard 0.1" header system was selected because a number of stack heights are possible and when combined with a standard standoff mounting system, ensures that the two boards are stacked securely.
- Multiple pins were allocated to the 24V rail to share the current carrying load. Due to the size of the 5V regulator and excess capacity available, the 5V rail is shared between the two boards.

## EtherCAT

The master control board also provides the necessary hardware to communicate via *EtherCAT*. The *EtherCAT* implementation, shown in Table 4.13, closely follows the *Microchip* reference implementation [Mic16]. *QSPI* was selected in favour of standard *SPI* to take advantage of the *QSPI* capabilities of the microcontroller to provide increased throughput, which will enable larger communication payloads in the future, if required.

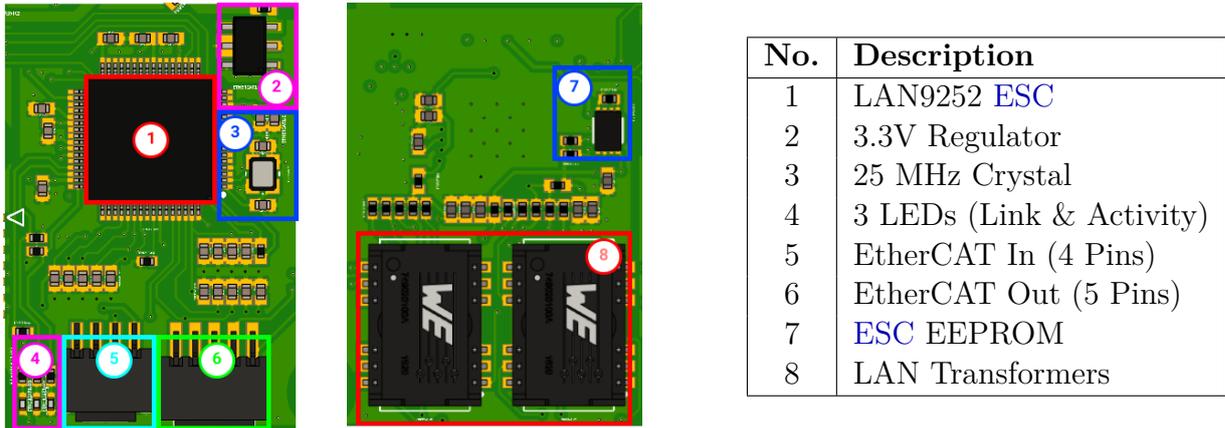


Figure 4.13.: Top and bottom view of EtherCAT Block

A summary of the important implementation features are provided below:

- A dedicated 3.3V regulator was used for *EtherCAT* section to minimise switching noise on the upstream power rails. The *LAN9252* has built in regulators to generate the other voltage rails required for operation.
- A *Molex PicoSPOX* 4 and 5 pin connector arrangement was used to maintain compatibility with other *EtherCAT* devices developed at *MIRMI*. This prevents incorrect wiring when connected in a line topology.
- *QSPI* communication interface is implemented and features protection resistors on the signal lines. Communication was tested at 6MHz clock frequencies.
- The sync line from *ESC* was connected to an interrupt capable pin on the microcontroller to allow for data latching required for distributed clock operation to ensure bus synchronisation.
- Three status LEDs were used to indicate connection status and help with diagnosing communication issues.

## Motor Driver

The motor driver implementation closely follows the implementation used by the motor control expansion board provided by MIRMI, including the fault latching circuit, over current monitor, current sensor configuration and Hall sensor signal conditioning. The calculations related to the fault latching circuit are provided in Appendix C. The overall implementation used for each motor is shown in Table 4.14.

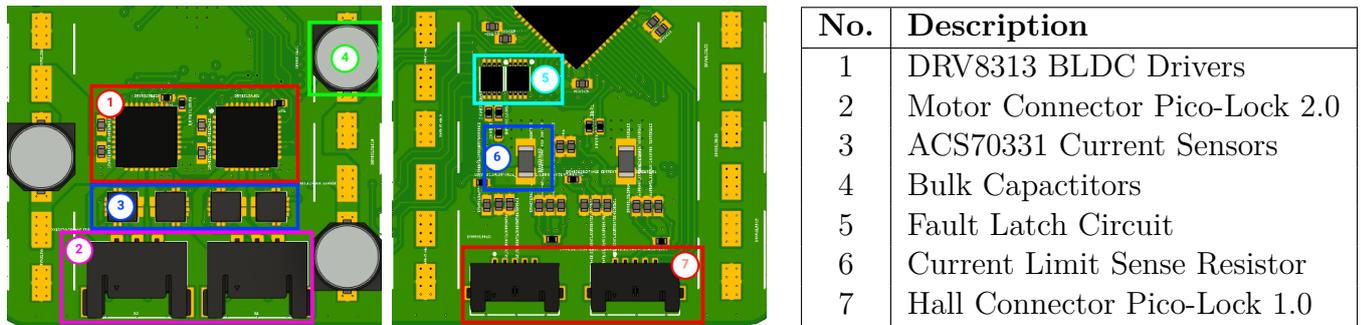


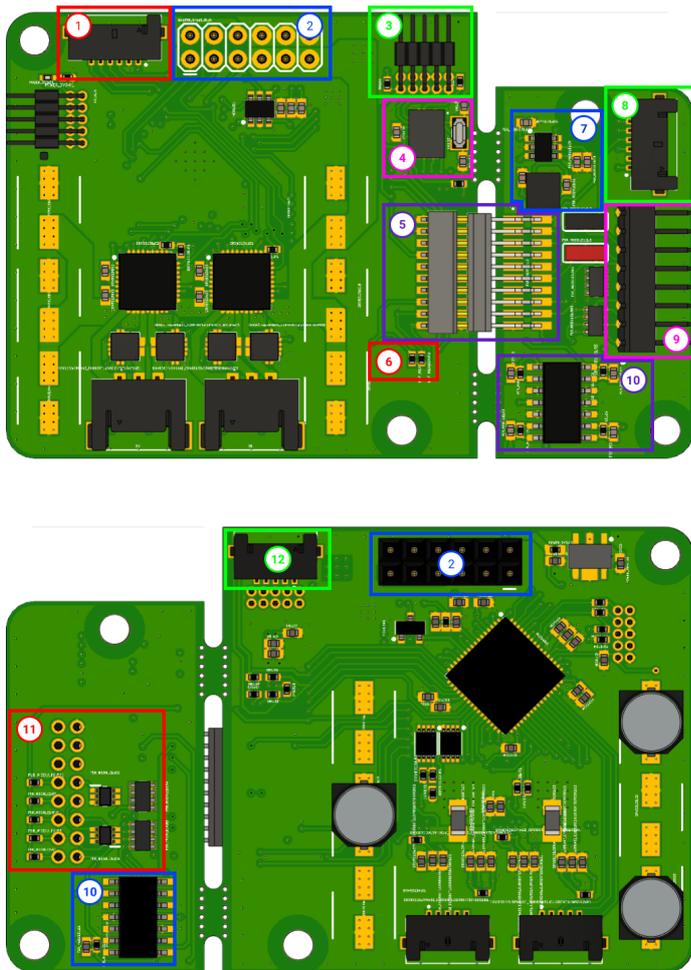
Table 4.14.: Top and bottom view the motor driver section

A summary of the other important implementation features is provided below:

- The motor Hall sensors require pull-up resistors for reliable edge transitions to be registered. Using the internal pull-up resistors in the microcontroller proved to be unreliable at higher speeds.
- Bulk local capacitance is provided for the connected motors. This aims to maintain stable motor voltages when high currents are required quickly. Only three of these capacitors are usually installed in an alternating arrangement to allow the master and slave control boards to be stacked.
- Finding appropriate connectors for the motors was not a trivial task. Compact, low profile and secure connectors with high current handling proved challenging to find. The *Molex Pico-Lock* series of connectors was one of few which fulfilled the requirements allowing for a lower stack height, while still being rated for up to 6A of current.

### 4.6.3. Slave Control Board (SCB)

The **SCB** shares the same basic **PCB** layer stack, motor control implementation and overall dimensions of the master control board to facilitate the stacked design. However, the *EtherCAT* and power protection features are not duplicated. Instead, the slave controller is responsible for providing the **IMU** functionality and analogue sensor interface via an alternate detachable expansion interface. An overview of the slave controller board is shown in [Table 4.15](#).



No.	Description
1	Angle Sensor Connector
2	Master Slave Interface
3	IMU Programming Header
4	IMU
5	Sensor Expansion Interface
6	Optional I2C pullup Resistors
7	Voltage Ref and Inverter
8	I2C or SPI expansion Header
9	Analog Sensor Connector
10	Trans-impedance Op-Amp
11	Analog Input Protection
12	Optional I2C header

**Note:**

Unlabelled items are common with Master

Table 4.15.: Top and bottom view of Slave Control Board

### Analogue Expansion Board

The required **FSR** signal conditioning circuitry outlined in [4.5.6](#) and additional digital interfaces are implemented on a breakaway expansion board shown in [Figure 4.14](#). This design was chosen to allow the flexibility of replacing the analogue sensor implementation to suit future platform requirements without the need to re-design the rest of the board. The additional digital interface could be used for additional digital sensors or analogue channels via an external **ADC**. The connector pin configuration and dimensional information needed when developing future expansion boards is provided in [Appendix D](#).

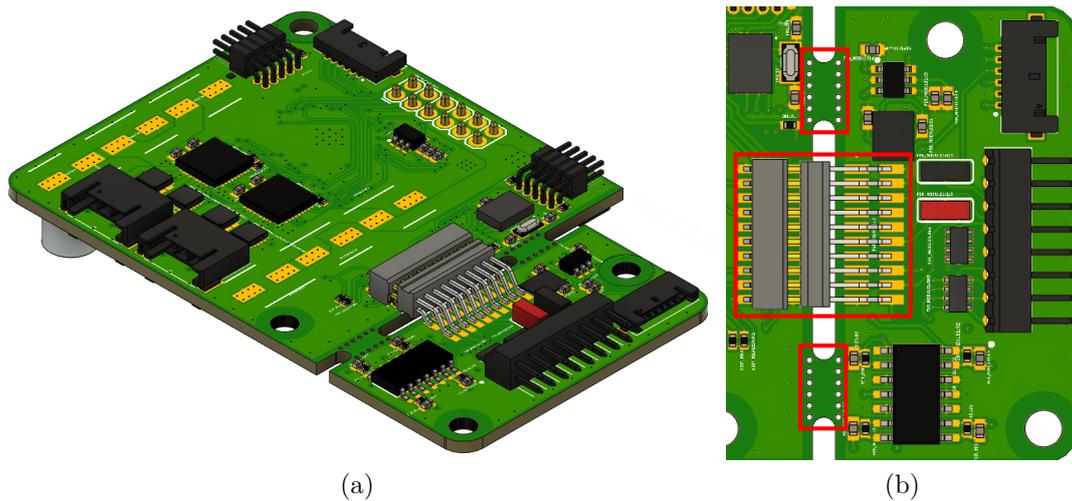


Figure 4.14.: (a) Slave Control Board (b) Expansion board breakaway section

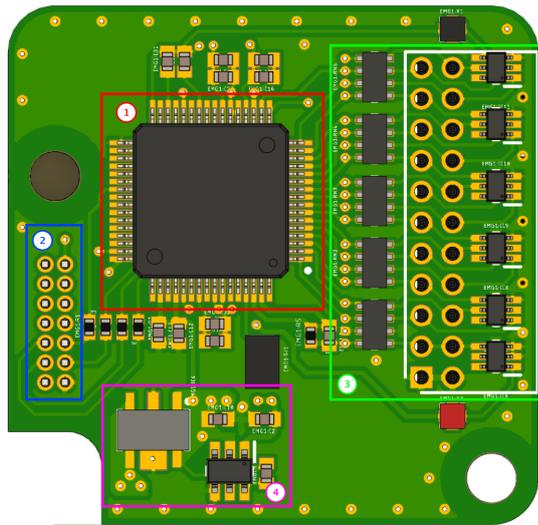
### Inertial measurement unit (IMU)

The **IMU** implementation was developed for the *BNO055* and *BMF055* range of sensors. The implementation closely follows the reference circuit provided in the datasheet [Bos11]. The development of custom motion sensing and sensor fusion firmware is out of the scope of this thesis, therefore the *BNO055* sensor was installed and tested with the in-house library developed at **MIRMI**. A summary of the other important implementation features is provided below:

- The recommended  $32.768kHz$  crystal oscillator is included.
- A 10-pin programming header is included which is the same as the header used for the main microcontroller and can be programmed using the same development tools.
- The **IMU** is configured to operate in I2C Mode with  $0x28$  address and the required pull-up resistors on the data lines are provided.
- An additional I2C header connected to the same bus as the **IMU** is provided for future expansion and debugging purposes.

#### 4.6.4. EMG Expansion Board

The **EMG** expansion board is responsible for the acquisition of the **sEMG** signals required to implement a **HMI**. The design was inspired by the *ADS1299EEGFE-PDK* [Tex16] and open source *OpenBCI Cython* [Ope] hardware. A two layer **PCB** design was used which complies with the expansion board form factor outlined in [Appendix D](#). An overview of the **EMG** expansion board is shown in [Table 4.16](#) and the design is intended to be used with with the electrode harness presented in [4.5.5](#) and snap on, disposable, adhesive gel electrodes.



No.	Description
1	ADS ASIC
2	Expansion interface Connector
3	Input Protection and filtering
4	3.3V regulator and Voltage inverter IC
5	+2.5V and -2.5V Regulator
6	Electrode connector
7	Decoupling Capacitors

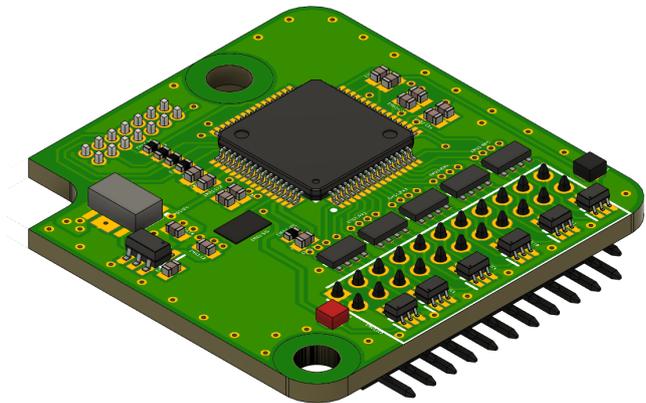
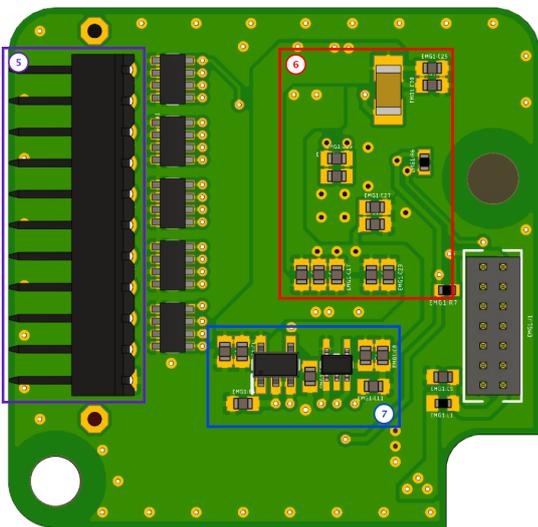
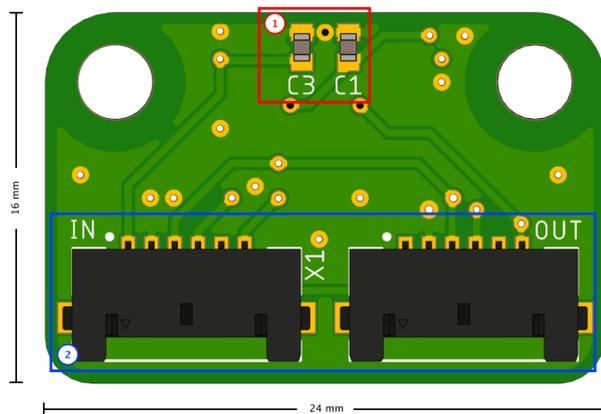


Table 4.16.: EMG Expansion Board

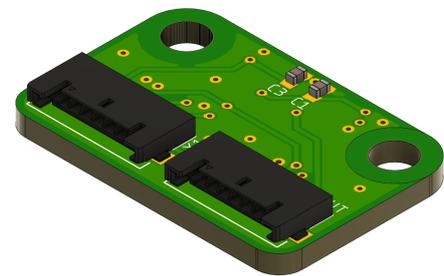
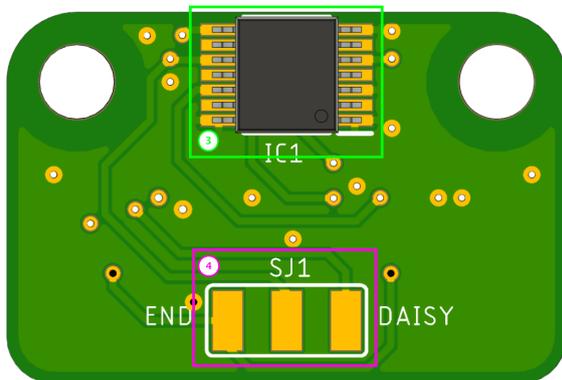
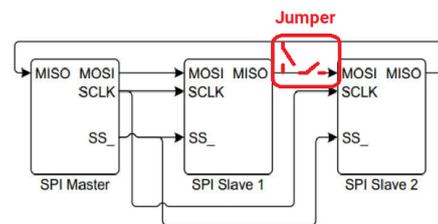
The *ADS1299* incorporates all commonly required features for **EMG**, including on-board reference generation, programmable gain, filtering and simultaneous conversion of up to eight input channels. The internal reference and oscillator were used in favour of providing these externally. Configuration and transfer of conversion data occurs via the **SPI** interface register; the required configuration settings adopted are documented in [Appendix E](#).

### 4.6.5. Absolute Angle Sensor Boards

Two different absolute angle sensor boards were developed to test the performance of the *A1335* and the *AS5048* sensors. As the mechanical configuration of the future prosthesis is unknown, a use case was adopted where the dipole target permanent magnets were attached directly to the motor shaft, instead of the driven end attached to the *DOF* as would normally be the case. The *PCBs* are based on a 2 layer design and the mounting holes were aligned with the sensor axis to correctly position the sensor. The functionality of the *A1335* and the *AS5048* are very similar, but the *A1335* supports off-axis sensing. A overview of the angle sensor boards and the relevant features discussed previously is shown in [Table 4.17](#).



No.	Description
1	Decoupling Capacitors
2	Sensor connector
3	Angle Sensor IC
4	Configuration Jumper



**Note:**

A1335 Board Shown, AS5048 board shares same dimensions

Table 4.17.: Angle Sensor Board

The angle sensors are intended to operate in a daisy-chain configuration, as such they feature an input and output connector. The hardware needs to be configured to match the desired sensor arrangement. This is done by installing a  $0\Omega$  jumper in the appropriate position as shown in [Table 4.17](#).

### 4.6.6. Assembled Prototype

The fully assembled platform is shown in Figure 4.15. The design requirements outlined in 4.1 stated that the platform developed shall be as space efficient as possible and smaller than the previous electronic platform used in the *CyberTUM* prototype, while adding the new functionality required. The dimensions for the platform developed is compared to the the previous *CyberTUM* prosthesis in Table 4.18. As shown, it is evident that the overall dimensions of the new platform developed are equivalent to just one of the two types of control boards used in the *CyberTUM* prototype. This was achieved while also providing two additional DOA, improving the motor control implementation, adding improved protection features and supporting additional sensors.

Component	Qty Required	Dimensions (mm)			Volume
		Length	Width	Height	Total ( $cm^3$ )
<b>This Work</b>					
Master Control Board	1	74	45	13	43.2
Slave Control Board	1	74	45	6	19.9
<b>Total</b>					63.1
<b>TUM Cybathlon Prosthesis</b>					
BLDC Board	2	85	40	18	61.2
Sensor Board	1	85	40	18	61.2
<b>Total</b>					183.6
<b>Size Reduction</b>					290%

Table 4.18.: Dimensional Comparison

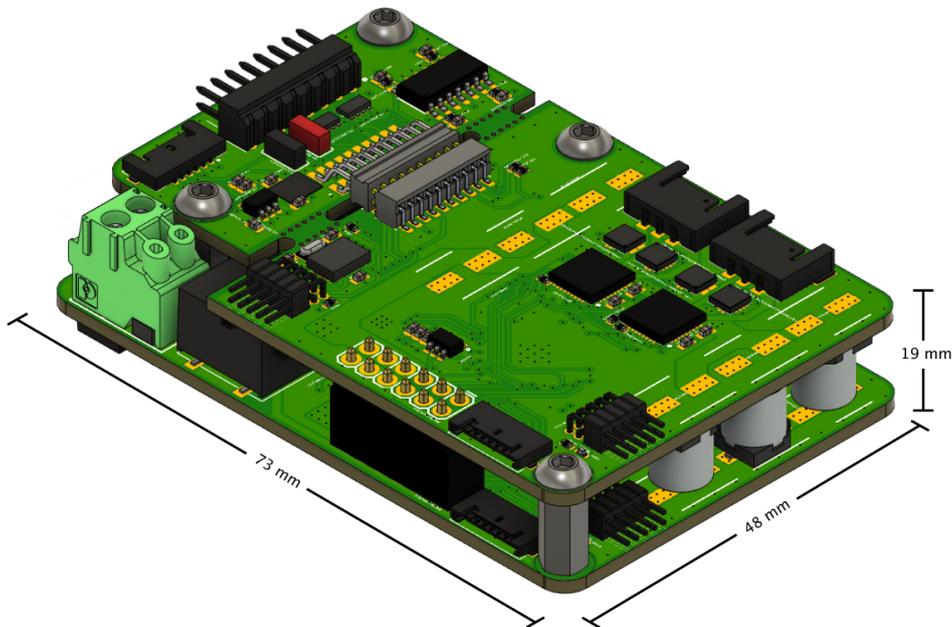


Figure 4.15.: Fully Assembled Platform

## 4.7. Firmware

This section provides an overview of the firmware implementation needed to operate the diverse hardware elements and facilitate tasks such as motor control, sensor feedback and real-time communication. The firmware makes extensive use of DMA features to perform peripheral to memory and vice versa transfers. Events and hardware timers are used to minimise the amount of interrupts required and free up the processor to focus on the high priority control tasks.

### 4.7.1. Block Diagram

A block diagram of the platform developed is presented in Figure 4.16 and provides an overview of the components, signals and microcontroller peripherals involved. The implementation is a continuation of the structure developed in chapter 3 and has been expanded to include two actuators per microcontroller and support the various additional sensors selected in Table 4.1.

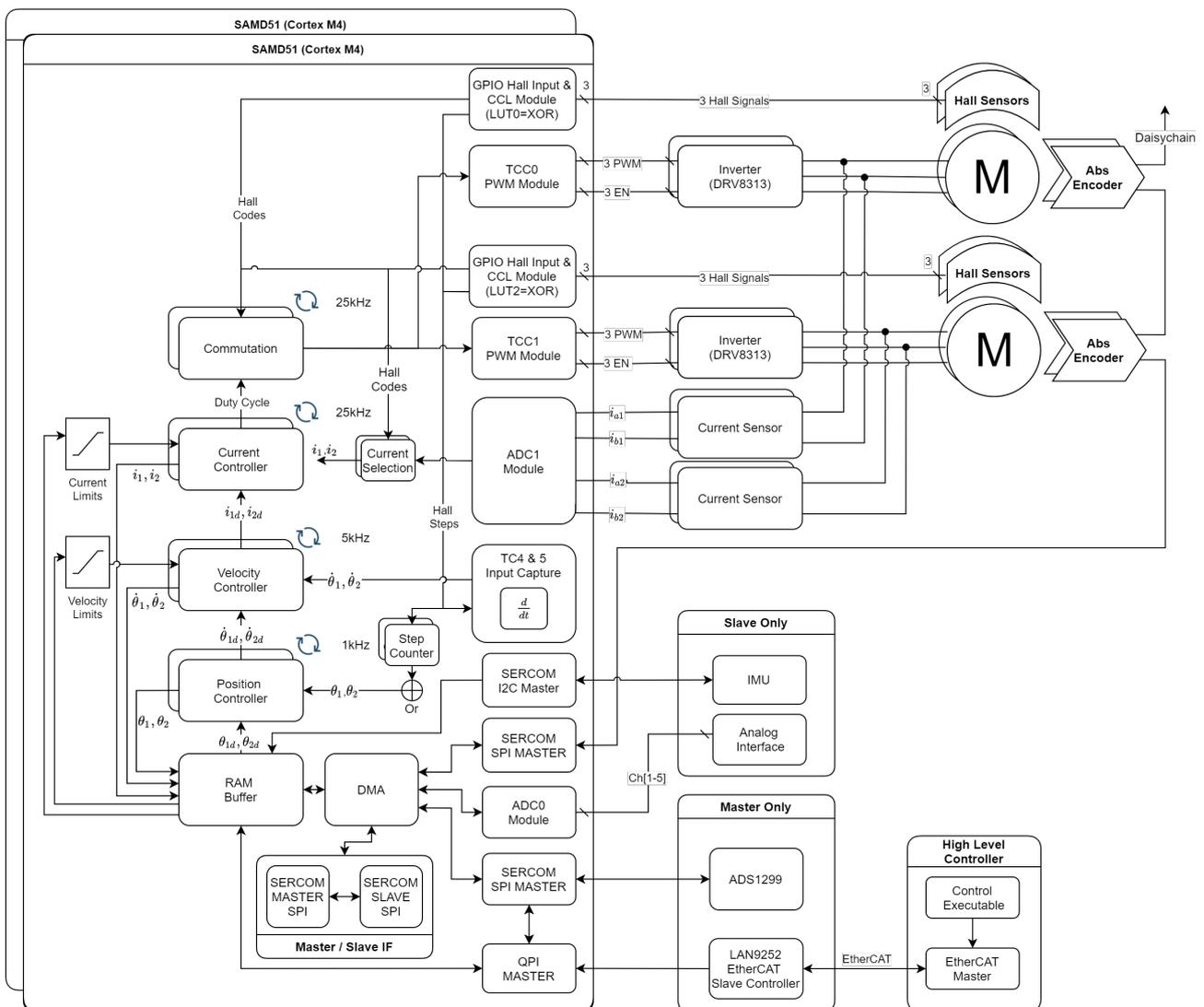


Figure 4.16.: Platform Block Diagram

## 4.7.2. Firmware Configuration

The firmware developed has been structured to make use of a single project for both the [MCB](#) and [SCB](#). The hardware was configured using the *Atmel Start* web based tool to configure the majority of the required peripherals and events visually. The generated drivers were used to initialise the required peripherals. This approach minimised code duplication and ensured implementation consistency. The required functionality was configured at compile time using pre-processor directives such that only the required source code was compiled and the hardware was configured according to the functionality distribution, as shown in [Figure 4.18](#).

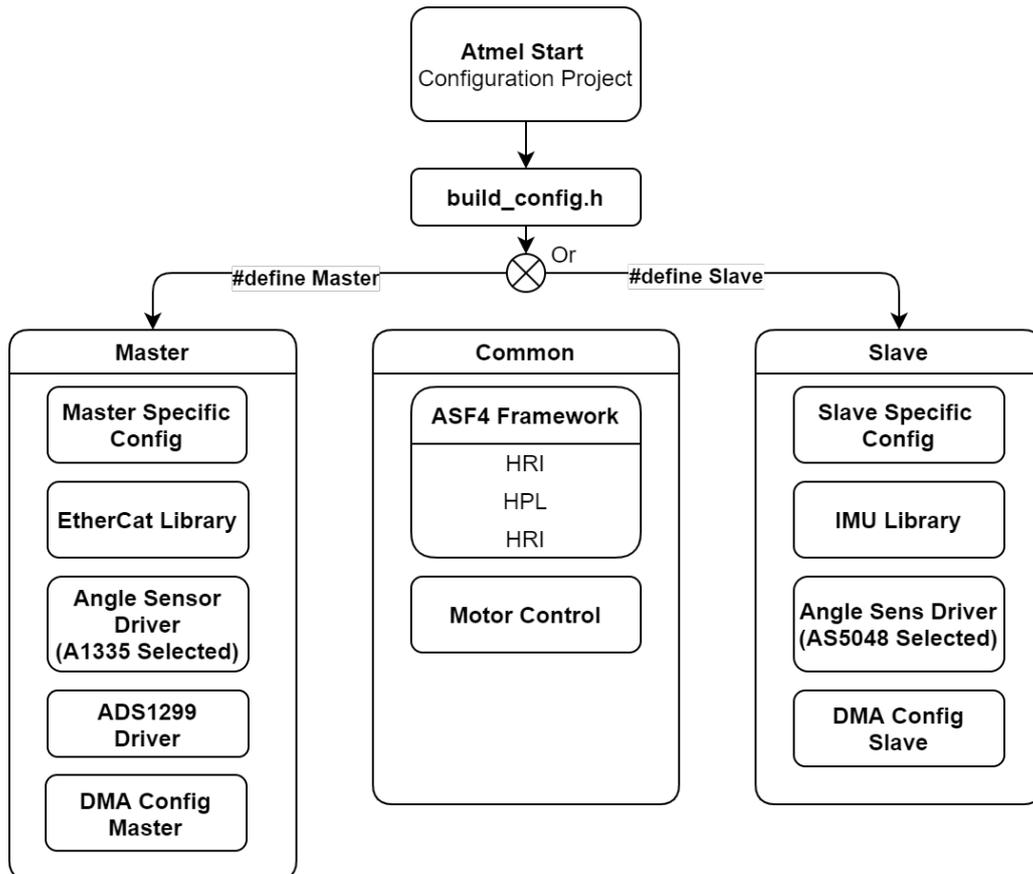


Figure 4.17.: Firmware Compile Time Configuration

### 4.7.3. Hardware Initialisation

The firmware performs the required hardware initialisation based on the configuration selected, as shown in the previous section. Once the DMA based tasks are configured, they can run continuously in the background without interrupting the main program and simply access a share section of memory. The remaining functionality is implemented in separate state machines which are called cyclically in the main loop.

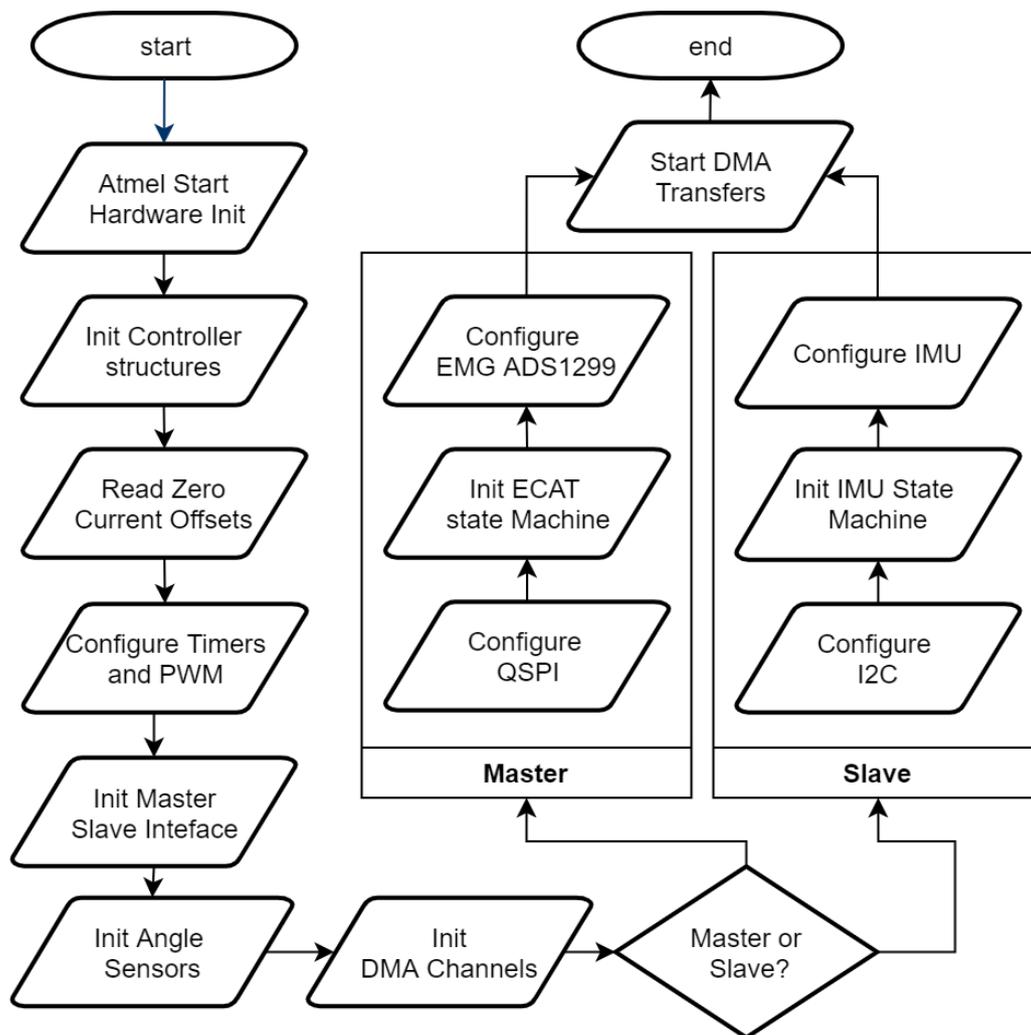


Figure 4.18.: Firmware Compile Time Configuration

### 4.7.4. Timing & Function Diagrams

The firmware operates in two distinct time domains. Motor control functionality is synchronised to the *PWM* cycle and the required software executes within one *PWM* cycle. The other is the *EtherCAT* time domain which, in this case, is  $1kHz$ . Data sent and received via *EtherCAT* needs to be acquired and processed with the one *EtherCAT* cycle.

### Motor Control Time Domain

The hardware, events and interrupts involved with motor control are shown in Figure 4.19. The PWM cycle triggers the ADC conversion needed for current control. Once the sampling is completed, a flag is set using an interrupt. Based on the state of this flag, all subsequent motor commutation and control tasks are processed sequentially. The tasks outlined are completed within the one PWM cycle, however the speed and position control run at differing frequencies. Only the worst case scenario, where all three execute sequentially, is shown.

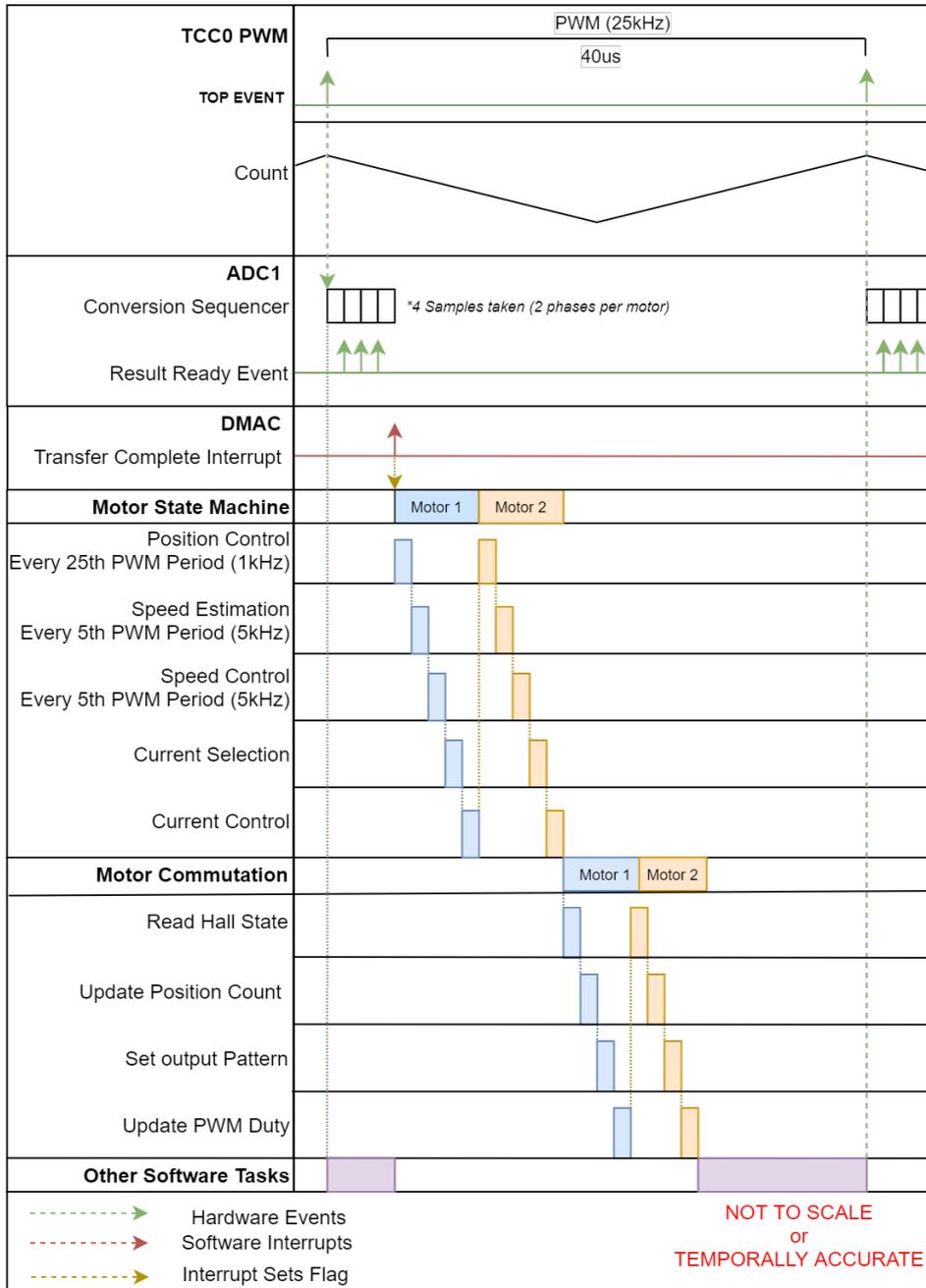


Figure 4.19.: Motor Control Timing Diagram

### EtherCAT Cycle Time Domain

The hardware, events and interrupts involved with *EtherCAT* cycle are shown in Figure 4.20. The timer triggers the required DMA transfers which then occur based on the established channel priority. An interrupt is triggered by the timer which sets a flag used to trigger the *EtherCAT* and IMU state machines responsible for transferring the data. The remaining transfers occur in the background and pending channels are blocked until the higher priority transfers have completed.

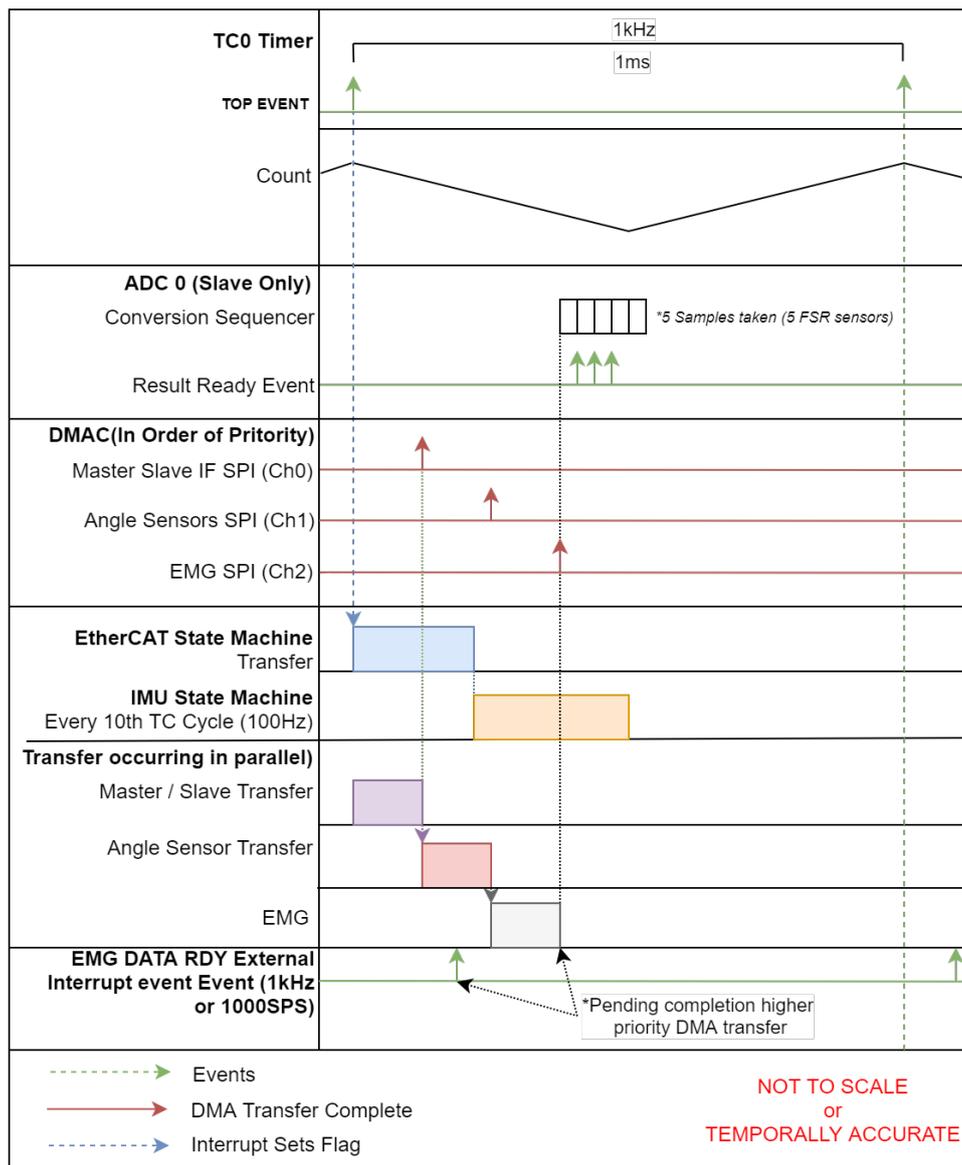


Figure 4.20.: Motor Control Timing Diagram

### 4.7.5. Serial Communication

Serial communication interfaces are responsible for a significant portion of the data transfer between controllers and sensors. As such, the implementation method of these transfers has an impact on the performance of the overall system. One of the strengths of the selected *SAMD51* microcontroller is the flexible serial communication interface which supports up to six hardware instances and can be configured to support a variety of protocols in both master and slave configurations.

#### Driver Implementations

The *Atmel Start* configuration tool provides several driver implementations to simplify configuration and usage of most hardware. The synchronous/blocking implementation is the simplest and is usually acceptable during startup for configuring serial peripherals, but blocking operations are not recommended on a platform running control loops and other "time critical" tasks relying on determinism. The asynchronous, or interrupt based, implementation eliminates the polling behaviour. However, full duplex serial protocols, such as *SPI*, are reliant on precise timing and factors, such as interrupt latency, can result in data corruption, especially at high clock rates. Transfer sizes and frequency can also affect overall system performance as the CPU interrupt mechanism introduces overheads which affect other time critical processes.

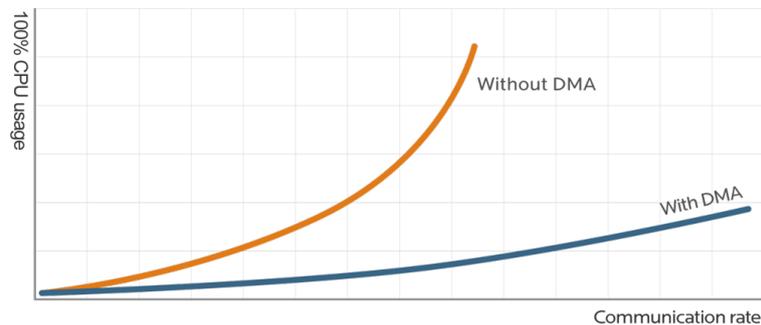


Figure 4.21.: Illustration of theoretical performance differences [Mic]

*DMA* based implementations can significantly improve overall system performance by freeing up the CPU from duties, such as memory transfers. The advantages of *DMA* are particularly pronounced at high communication rates and larger data transfers, as shown in [Figure 4.21](#). *DMA* based implementations were used where possible to take advantage of these benefits, despite the additional complexity introduced.

A summary of the *SPI* transfers, which have been implemented using *DMA* and require no CPU intervention, are shown in [Table 4.19](#). These transfers were good candidates as they occur in a cyclic fashion and would likely have significantly impacted overall performance if a synchronous or interrupt based implementation was used. Ideally, the *EtherCAT* and *IMU* communication channels would also be converted to *DMA* operation, however due to time constraints, this was not completed.

Peripheral	Description	Transfer Size (Bytes)	Baud Rate (MHz)	Transfer Freq (KHz)
SERCOM1	Board to Board(Master/Slave) <sup>1</sup>	64	4	1
SERCOM2	EMG (ADS1299) <sup>2</sup>	27	2	1
SERCOM5	Angle Sensors	4	1	1

<sup>1</sup> Different implementation for Master and Slave

<sup>2</sup> Only for Master Board

Table 4.19.: SPI DMA Transfers

### Event Based CS handling

For successful SPI communication, the master must control the CS pin and data lines in a manner that is compatible with each slave attached on the bus. As previously stated, avoiding interrupts and taking advantage of hardware based events was important to ensure accurate timing and that synchronisation was maintained. Toggling the CS line in software is prone to jitter and is a waste of CPU resources. The Port IO controller of the microcontroller allows for events to set, clear and toggle IO pins without intervention from the CPU. Using a separate set and clear event for each pin would only allow two CS pins to be controlled.

A solution implemented was to use the compare channels of a timer to both output a PWM waveform and trigger a DMA transfer. The resulting waveform was then combined with an event using the CCL hardware built into the microcontroller which allows for a logical XOR operation to be performed on the two input signals. The rising edges of the XOR result can then be used to trigger the toggling of the desired IO pin. This solution, illustrated in Figure 4.23, allows up to four CS pins to be controlled precisely, independent of the CPU. The timing between transfers and delay between dropping the CS pin and starting a transfer using DMA can be precisely controlled to ensure minimum timing requirements, such as  $t_{SSS}$  shown in Figure 4.22, can be adapted to suit the slave.

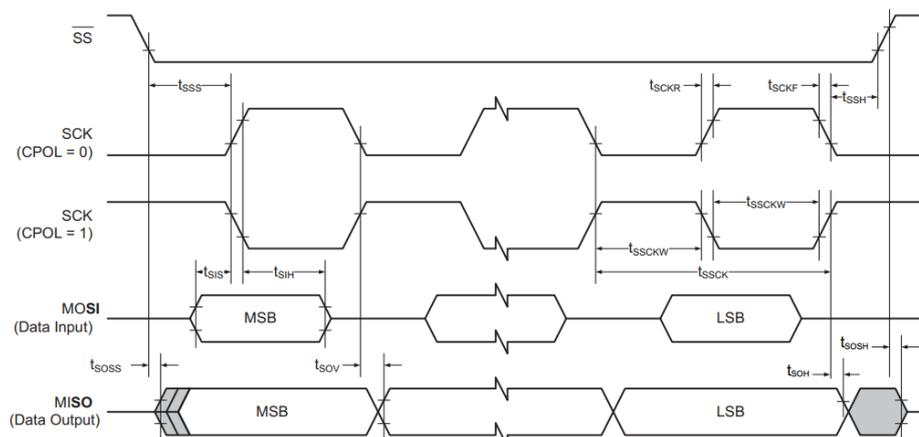


Figure 4.22.: SPI Timing Requirements [Mic10]

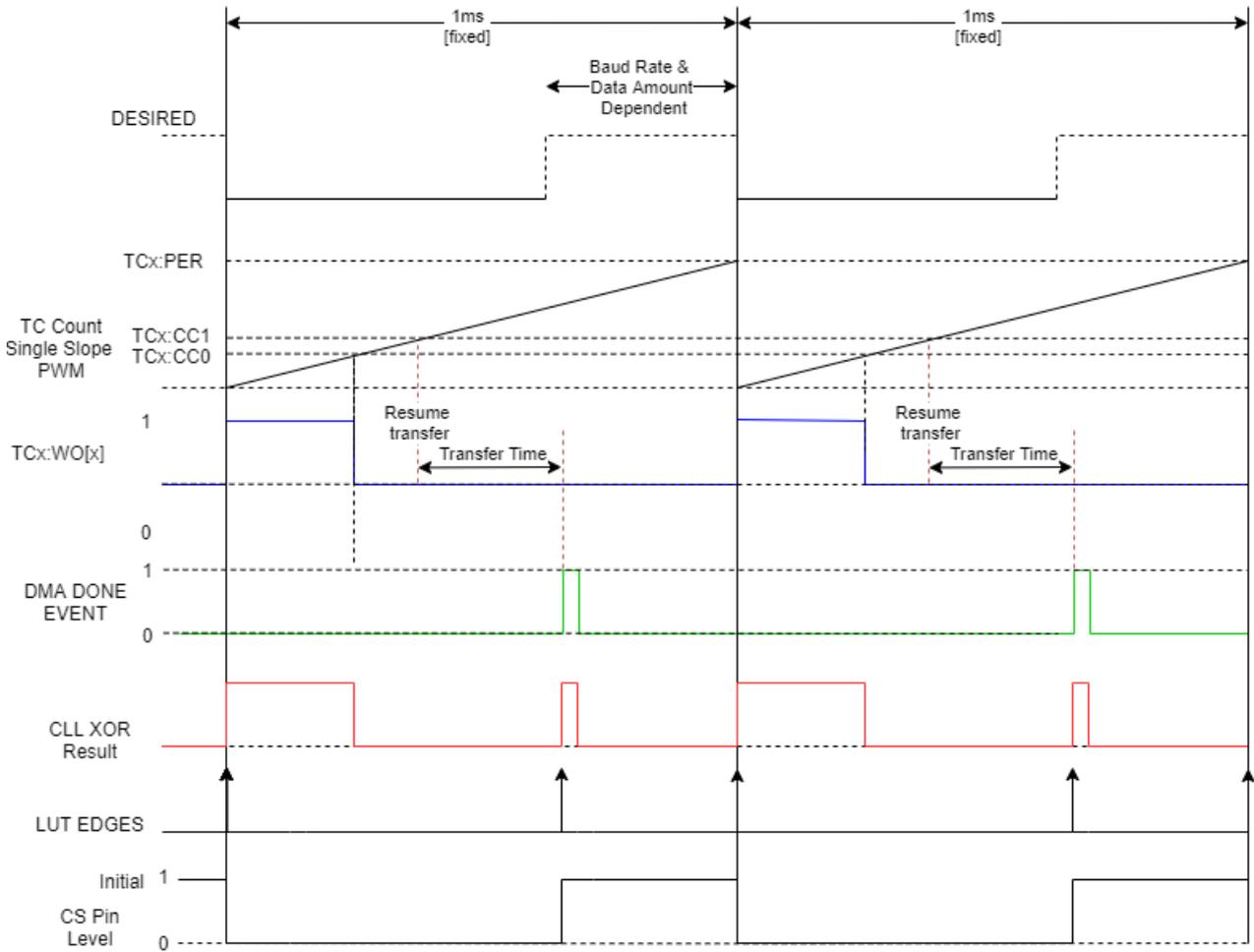


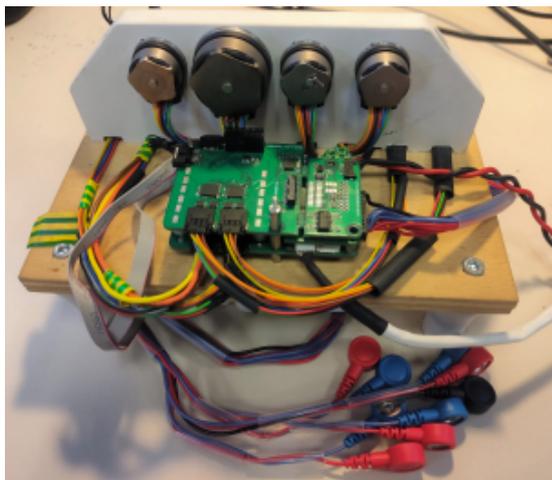
Figure 4.23.: DMA CS Handling

# 5. Evaluation & Results

In order to evaluate the hardware and firmware developed, the prototype needed to be tested extensively to obtain the required performance data. This section presents the test bench that was developed and the data and results obtained for the various components developed.

## 5.1. Test Bench

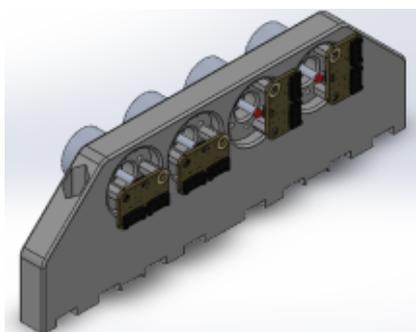
Following the fabrication and assembly of the various circuit boards developed, the compact test bench shown in [Figure 5.1](#) was developed to securely mount all the components. The motors and corresponding angle sensors are attached to a 3D printed structure which allows the motors to rotate freely, load disturbances were usually simulated using a finger.



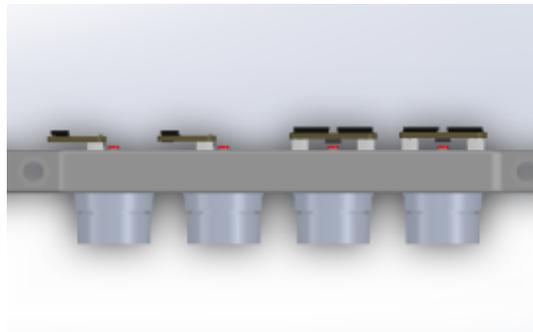
(a)



(b)



(c)



(d)

Figure 5.1.: (a) Test Bench (b) Underside (c) Angle Sensor Mounting (d) Top View

The on-axis and off-axis angle sensing configurations were tested using the mounting points provided. These were designed to position the sensor in range of the required dipole magnet (shown in red) in Figure 5.1c and 5.1d. As no gearbox was used, the magnets were attached directly to the motor shaft to simulate placement on the link side.

The underside of the test bench is used to mount the required *Atmel-ICE* debugging and programming adaptors connected to the MCB and SCB to allow both controllers to be programmed and debugged simultaneously. Additionally, the bench provides the necessary strain relief for the various cables and sEMG electrode harness. A provision was made to mount a Single Board Computer (SBC) single board computer, such as raspberry pi or beagle board, to test the implementation of a SBC based high level controller, but this remains as possible future work.

## 5.2. Data Acquisition & Testing

The test bench was used in conjunction with *TwinCAT* during the development and data acquisition phase to transmit set-points and obtain readings at  $1kHz$  over *EtherCAT*. This section introduces the various tests performed and the results obtained to demonstrate the functionality of the electronic platforms various components working together. Unfortunately, a hardware failure that could not be resolved in time for the submission deadline, resulted in the desired level of evaluation data being impossible to obtain. The results presented are based on the data that was available and recorded during development and could, unfortunately, not be reformatted in a more appropriate format.

### 5.2.1. Motor Control

In addition to the motor control related data obtained in chapter 3, which focused on controller specific performance based on a single actuator, this section evaluates the cascaded control performance of all four actuators simultaneously with higher level position based path tracking and enforced current and velocity limits. *TwinCAT* was used to generate a commanded position profile and the resulting response was observed.

To confirm the motor control functionality, a coordinated motion test was performed, the same position profile was provided to all four actuators (indicated in *blue*). The resulting motor position and current response (*green* and *red*, respectively) is shown in Figure 5.2. The results reveal that all actuators follow the commanded profile and the acceleration and deceleration ramps highlight the speed and current limits imposed by the cascaded controllers.



Figure 5.2.: Motor Trace

### 5.2.2. EMG Data

The sEMG data is obtained from the *ADS1299* in a cyclic fashion via the *SPI* interface. The *ADS1299* features a built-in test pattern generator whose output can be routed to each of the input channels to verify that the *AFE*, conversion stage and communication to the host microcontroller are working correctly. The square wave test signal is configurable in amplitude ( $\pm 1mV$  or  $\pm 2mV$ ) as well as frequency ( $1Hz$  or  $2Hz$ ). The test signal generator was configured to  $\pm 1mV$  and  $1Hz$ . The resulting data was scaled and successfully reproduced the expected test signal as shown in [Figure 5.3](#), indicating that the implementation is working correctly. Unfortunately, testing on a human subject was not possible in the time remaining.

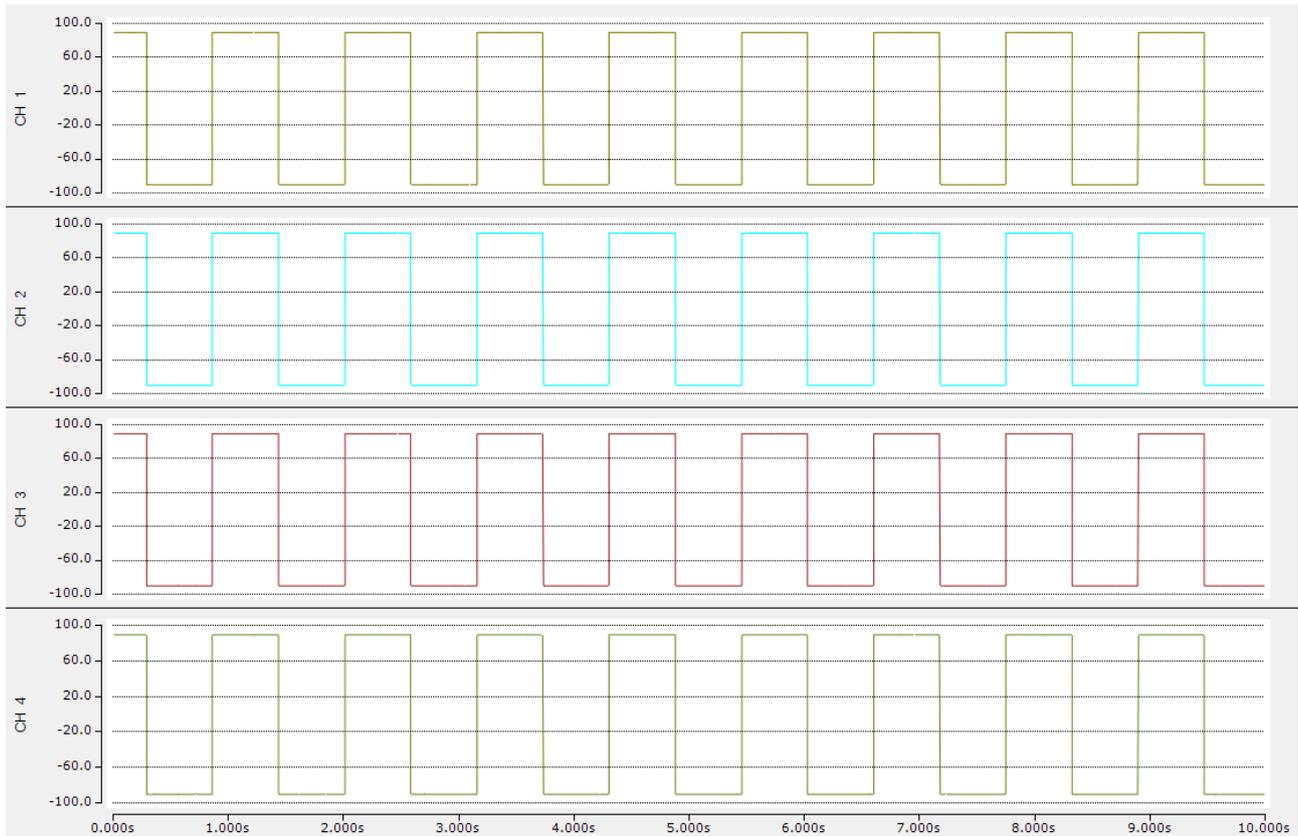


Figure 5.3.: EMG Test Pattern

### 5.2.3. Remaining Sensor Data

The data from the remaining sensors was successfully obtained during development, however the data captured was no longer available. As such, the desired data graphs could not be included. A description of the data is still provided.

The fused sensor data is obtained from the [IMU](#) in quaternion format. This avoids the issues of gimbal lock traditionally associated with the Euler angle representation but is less intuitive to understand. The data consists of four variables in a 16-bit signed format which needs to be scaled accordingly.

The daisy-chain implementation of the angle sensors was tested by rotating the motors by hand to a desired position and then rotating back to the start position. This testing revealed that, unfortunately, the *A1335* does not support the daisy-chain configuration and only the first sensor in the chain provided a valid reading, however the off-axis capabilities of the sensor were confirmed. The *AS5048* sensors functioned as expected.

# 6. Conclusion & Future Work

## 6.1. Conclusion

This thesis presented the design of an embedded electronic platform which is intended for use by students of the *Cyathlon* project course offered at [TUM](#) to develop an improved trans-radial prosthesis, in the lead up to the 2024 *Cyathlon* Competition. The design of the new platform was based on the analysis of limitations of the current electronics platform used for the 2020 competition, as well as the current state-of-the-art commercial and research prostheses. The limitations identified were addressed and new desirable features were incorporated into the platform design and a functional prototype was fabricated.

In addition to the hardware developed, the firmware and drivers necessary to operate the diverse hardware elements and facilitate tasks such as motor control, sensor feedback and real-time communication was also developed. The comprehensive electronics platform was then verified with the help of a test bench in lieu of an actual prosthesis.

The resulting electronics platform achieved a 290% reduction in electronics footprint from previous platform, while still providing additional features and supporting four [BLDC](#) Motors. The motor control implementation, [EMG](#), digital and analogue sensor implementation have also been improved. The flexible design provides defined expansion interfaces which can be used to customise the features supported by the platform without affecting the core motor control and communication functionality. This approach addresses the need to minimise the re-design the electronics and the effort required to support new features or future prosthesis configurations.

The author believe that the provisions made in the design of this platform will empower future students to develop the next generation of *Cybertum* prosthesis with capabilities necessary to tackle the new challenges of 2024 *Cyathlon*.

## 6.2. Future Work

For the future, some additional effort will be necessary to make full use of the platform developed. The tasks expected are summarised in the following list:

- The control loops were tuned and tested without a load or gearbox attached. The controllers will require tuning to suit the intended application to achieve maximum performance
- Mechanical integration inside the new prosthesis will be necessary. The small footprint achieved should simplify the integration of the electronics with the prosthesis.
- The high level control implementation will need to be developed. Certain communication parameters and EtherCAT specific configuration will need to be adapted in the firmware provided.
- The application state machine and error handling in firmware implementation needs to be improved to ensure stability in all operating conditions.
- EMG interface requires more extensive testing with a human subject to confirm the configuration setting outlined in [Appendix E](#).
- The battery powered operation and safety features provided need to be tested. The platform was only tested in tethered operation.

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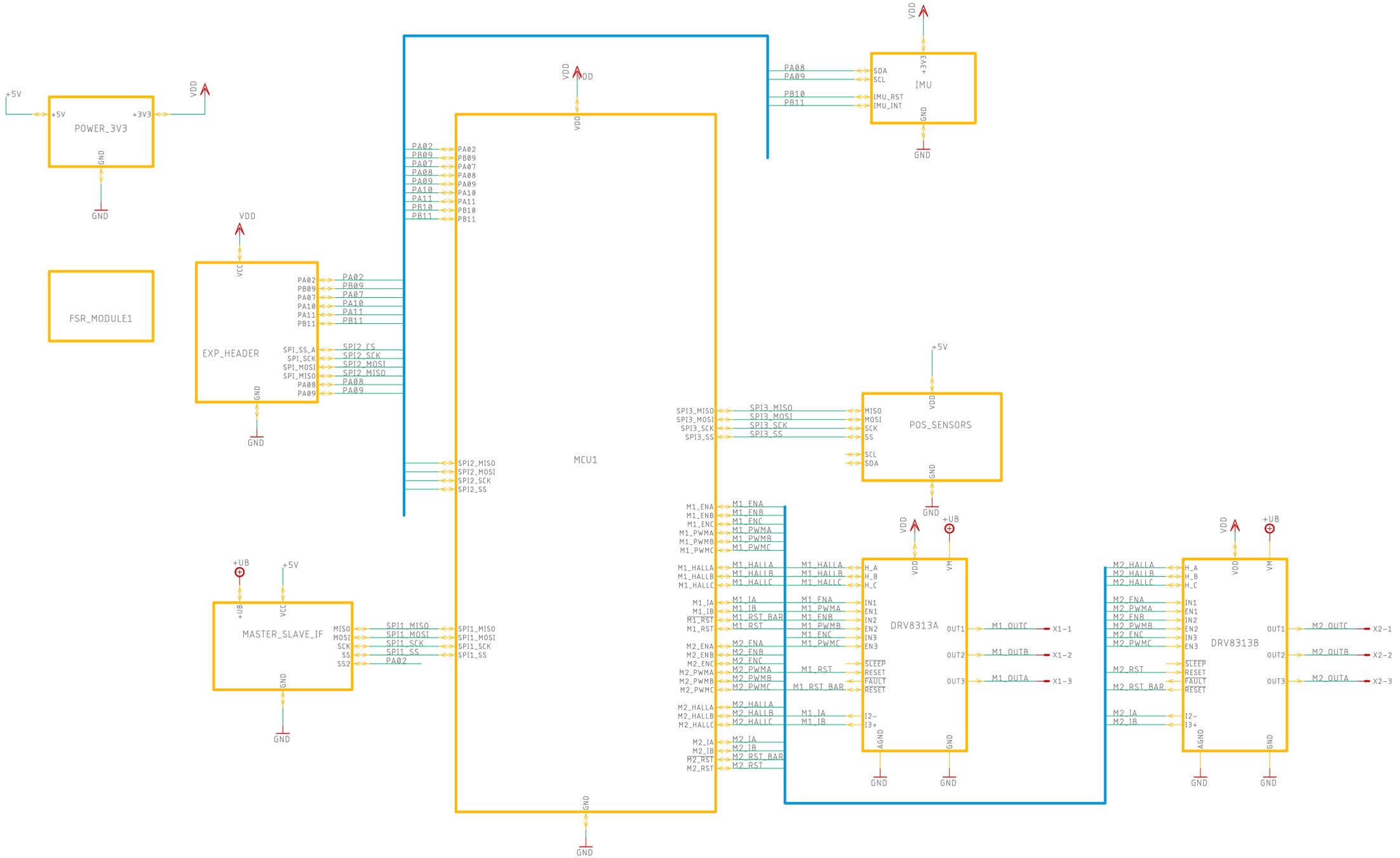


# A. Microcontroller Pin Allocations

Mater	Slave	VQFN 64	Pad Name	EIC	ANAREF	ADC0	ADC1	SERCOM	SERCOM	TCC	TCC, PDEC	QSPI	CCL
SPI1_MOSI	SPI1_MOSI	01/B8	PA00	EIC/ EXTINT[ 0]	-	-	-	-	SERCO M1/ PAD[0]	-	-	-	-
SPI1_SCK	SPI1_SCK	02/C8	PA01	EIC/ EXTINT[ 1]	-	-	-	-	SERCO M1/ PAD[11]	-	-	-	-
ADS Reset	ANLG_ADC0	03/C7	PA02	EIC/ EXTINT[ 2]	-	ADC0/ AIN[0]	-	-	-	-	-	-	-
ANAREF_2.024	ANAREF_2.024	04/D6	PA03	EIC/ EXTINT[ 3]	ANAREF /VREFEA	ADC0/ AIN[1]	-	-	-	-	-	-	-
M2_IB	M2_IB	05/D7	PB04	EIC/ EXTINT[ 4]	-	-	ADC1/ AIN[6]	-	-	-	-	-	-
M2_IA	M2_IA	06/D8	PB05	EIC/ EXTINT[ 5]	-	-	ADC1/ AIN[7]	-	-	-	-	-	-
M1_IB	M1_IB	09/E7	PB06	EIC/ EXTINT[ 6]	-	-	ADC1/ AIN[8]	-	-	-	-	-	CCL/ IN[6]
M1_IA	M1_IA	10/E6	PB07	EIC/ EXTINT[ 7]	-	-	ADC1/ AIN[9]	-	-	-	-	-	CCL/ IN[7]
Vref/2	Vref/2	11/F5	PB08	EIC/ EXTINT[ 8]	-	ADC0/ AIN[2]	ADC1/ AIN[0]	-	SERCO M4/ PAD[0]	-	-	-	CCL/ IN[8]
ADS Data Ready	ANLG_ADC0	12/F8	PB09	EIC/ EXTINT[ 9]	-	ADC0/ AIN[3]	ADC1/ AIN[1]	-	SERCO M4/ PAD[11]	-	-	-	-
M1_HALLA	M1_HALLA	13/F7	PA04	EIC/ EXTINT[ 4]	ANAREF /VREFB	ADC0/ AIN[4]	-	-	SERCO M0/ PAD[0]	-	-	-	CCL/ IN[0]
M1_HALLB	M1_HALLB	14/F6	PA05	EIC/ EXTINT[ 5]	-	ADC0/ AIN[5]	-	-	SERCO M0/ PAD[11]	-	-	-	CCL/ IN[1]
M1_HALLC	M1_HALLC	15/G7	PA06	EIC/ EXTINT[ 6]	ANAREF /VREFC	ADC0/ AIN[6]	-	-	SERCO M0/ PAD[2]	-	-	-	CCL/ IN[2]
ECAT SYNC	ANLG_ADC0	16/G8	PA07	EIC/ EXTINT[ 7]	-	ADC0/ AIN[7]	-	-	SERCO M0/ PAD[3]	-	-	-	-
ECAT_QSPI_MOSI	IMU_SDA	17/H8	PA08	EIC/NMI	-	ADC0/ AIN[8]	ADC1/ AIN[2]	SERCO M0/ PAD[0]	SERCO M2/ PAD[1]	-	-	-	QSPI/ DATA[0]
ECAT_QSPI_MISO	IMU_SCL	18/G6	PA09	EIC/ EXTINT[ 9]	-	ADC0/ AIN[9]	ADC1/ AIN[3]	SERCO M0/ PAD[1]	SERCO M2/ PAD[0]	-	-	-	QSPI/ DATA[1]
ECAT_QSPI_DATA2	ANLG_ADC0	19/H7	PA10	EIC/ EXTINT[ 10]	-	ADC0/ AIN[10]	-	SERCO M0/ PAD[2]	SERCO M2/ PAD[2]	-	-	-	QSPI/ DATA[2]
ECAT_QSPI_DATA3	ANLG_ADC0	20/G5	PA11	EIC/ EXTINT[ 11]	-	ADC0/ AIN[11]	-	SERCO M0/ PAD[3]	SERCO M2/ PAD[3]	-	-	-	QSPI/ DATA[3]
ECAT_QSPI_SCK	IMU_Reset	23/H6	PB10	EIC/ EXTINT[ 10]	-	-	-	-	SERCO M4/ PAD[2]	-	-	-	QSPI/ SCK
ECAT_QSPI_CS	IMU_interrupt	24/G4	PB11	EIC/ EXTINT[ 11]	-	-	-	-	SERCO M4/ PAD[3]	-	-	-	QSPI/ CS
M1_ENA (EN3)	M1_ENA (EN3)	25/H5	PB12	EIC/ EXTINT[ 12]	-	-	-	SERCOM4/ PAD[0]	-	TCC0/ WO[0]	-	-	-
M1_PWMA (IN3)	M1_PWMA (IN3)	26/H4	PB13	EIC/ EXTINT[ 13]	-	-	-	SERCO M4/ PAD[11]	-	TCC0/ WO[1]	-	-	-
M1_ENB (EN2)	M1_ENB (EN2)	27/G3	PB14	EIC/ EXTINT[ 14]	-	-	-	SERCO M4/ PAD[2]	-	TCC0/ WO[2]	-	-	CCL/ IN[9]
M1_PWM (IN2)	M1_PWM (IN2)	28/H3	PB15	EIC/ EXTINT[ 15]	-	-	-	SERCO M4/ PAD[3]	-	TCC0/ WO[3]	-	-	CCL/ IN[10]
SPI2_MOSI	SPI2_MOSI	29/F2	PA12	EIC/ EXTINT[ 12]	-	-	-	SERCO M2/ PAD[0]	SERCO M4/ PAD[11]	TCC0/ WO[6]	TCC1/ WO[2]	-	-
SPI2_SCK	SPI2_SCK	30/G2	PA13	EIC/ EXTINT[ 13]	-	-	-	SERCO M2/ PAD[11]	SERCO M4/ PAD[0]	TCC0/ WO[7]	TCC1/ WO[3]	-	-
SPI2_SS	SPI2_SS	31/H1	PA14	EIC/ EXTINT[ 14]	-	-	-	SERCO M2/ PAD[2]	SERCO M4/ PAD[2]	-	TCC1/ WO[2]	-	-
SPI2_MISO	SPI2_MISO	32/H2	PA15	EIC/ EXTINT[ 15]	-	-	-	SERCO M2/ PAD[3]	SERCO M4/ PAD[3]	-	TCC1/ WO[3]	-	-
M2_ENA (EN3)	M2_ENA (EN3)	35/G1	PA16	EIC/ EXTINT[ 0]	-	-	-	SERCO M1/ PAD[0]	SERCO M3/ PAD[11]	TCC1/ WO[0]	TCC0/ WO[4]	-	CCL/ IN[0]
M2_PWMA (IN3)	M2_PWMA (IN3)	36/F1	PA17	EIC/ EXTINT[ 1]	-	-	-	SERCO M1/ PAD[11]	SERCO M3/ PAD[0]	TCC1/ WO[1]	TCC0/ WO[5]	-	CCL/ IN[1]
M2_ENB (EN2)	M2_ENB (EN2)	37/E1	PA18	EIC/ EXTINT[ 2]	-	-	-	SERCOM1/ PAD[2]	SERCO M3/ PAD[2]	TCC1/ WO[2]	TCC0/ WO[6]	-	CCL/ IN[2]
M2_PWM (IN2)	M2_PWM (IN2)	38/E2	PA19	EIC/ EXTINT[ 3]	-	-	-	SERCOM1/ PAD[3]	SERCO M3/ PAD[3]	TCC1/ WO[3]	TCC0/ WO[7]	-	CCL/ OUT[0]
M1_ENC (EN1)	M1_ENC (EN1)	39/D4	PB16	EIC/ EXTINT[ 0]	-	-	-	SERCO M5/ PAD[0]	-	-	TCC0/ WO[4]	-	CCL/ IN[11]
M1_PWM (IN1)	M1_PWM (IN1)	40/D1	PB17	EIC/ EXTINT[ 1]	-	-	-	SERCO M5/ PAD[11]	-	-	TCC0/ WO[5]	-	CCL/ OUT[3]
M2_ENC (EN1)	M2_ENC (EN1)	41/D2	PA20	EIC/ EXTINT[ 4]	-	-	-	SERCO M5/ PAD[2]	SERCO M3/ PAD[2]	TCC1/ WO[4]	TCC0/ WO[0]	-	-
M2_PWM (IN1)	M2_PWM (IN1)	42/D3	PA21	EIC/ EXTINT[ 5]	-	-	-	SERCO M5/ PAD[3]	SERCO M3/ PAD[3]	TCC1/ WO[5]	TCC0/ WO[1]	-	-
M2_HALLA	M2_HALLA	43/C1	PA22	EIC/ EXTINT[ 6]	-	-	-	SERCO M3/ PAD[0]	SERCO M5/ PAD[11]	TCC1/ WO[6]	TCC0/ WO[2]	-	CCL/ IN[6]
M2_HALLB	M2_HALLB	44/C2	PA23	EIC/ EXTINT[ 7]	-	-	-	SERCO M3/ PAD[11]	SERCO M5/ PAD[0]	TCC1/ WO[7]	TCC0/ WO[3]	-	CCL/ IN[7]
M2_HALLC	M2_HALLC	45/B1	PA24	EIC/ EXTINT[ 8]	-	-	-	SERCO M3/ PAD[2]	SERCO M5/ PAD[2]	-	-	-	CCL/ IN[8]
M2_RST_Bar	M2_RST_Bar	46/A1	PA25	EIC/ EXTINT[ 9]	-	-	-	SERCO M3/ PAD[3]	SERCO M5/ PAD[3]	-	-	-	CCL/ OUT[2]
SPI1_CS	SPI1_CS	49/A2	PB22	EIC/ EXTINT[ 6]	-	-	-	SERCO M1/ PAD[2]	SERCO M5/ PAD[2]	-	-	-	CCL/ IN[0]
SPI1_MISO	SPI1_MISO	50/A3	PB23	EIC/ EXTINT[ 7]	-	-	-	SERCO M1/ PAD[3]	SERCO M5/ PAD[3]	-	-	-	CCL/ OUT[0]
M2_RST	M2_RST	51/B3	PA27	EIC/ EXTINT[ 11]	-	-	-	-	-	-	-	-	-
M1_RST_Bar	M1_RST_Bar	59/A6	PB30	EIC/ EXTINT[ 14]	-	-	-	-	SERCO M5/ PAD[1]	-	TCC0/ WO[6]	-	-
M1_RST	M1_RST	60/B6	PB31	EIC/ EXTINT[ 15]	-	-	-	-	SERCO M5/ PAD[0]	-	TCC0/ WO[7]	-	-
SPI3_SS	SPI3_SS	61/A7	PB00	EIC/ EXTINT[ 0]	-	ADC0/ AIN[12]	-	-	SERCO M5/ PAD[2]	-	-	-	-
SPI3_MISO	SPI3_MISO	62/B7	PB01	EIC/ EXTINT[ 1]	-	ADC0/ AIN[13]	-	-	SERCO M5/ PAD[3]	-	-	-	-
SPI3_MOSI	SPI3_MOSI	63/A8	PB02	EIC/ EXTINT[ 2]	-	ADC0/ AIN[14]	-	-	SERCO M5/ PAD[0]	-	-	-	-
SPI3_SCK	SPI3_SCK	64/C6	PB03	EIC/ EXTINT[ 3]	-	ADC0/ AIN[15]	-	-	SERCO M5/ PAD[1]	-	-	-	-

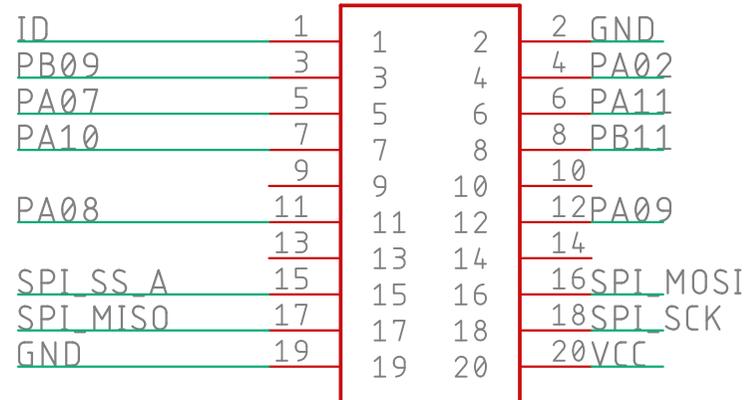
## **B. Schematics & Layouts**

# Master Control Board



# Master Control Board

1:ID	2: GND
3:ADC+	4: ADC-
5:GPIO1	6:GPIO2
7:PWM+	8:PWM-
9:IRQ	10:SPI_SSB
11:I2C_SDA	12:SI2C_SCL
13:USART_TX	14:USART_RX
15:SPI_SSA	16:SPI_MOSI
17:SPI_MISO	18:SPI_SCK
19:GND	20:VCC

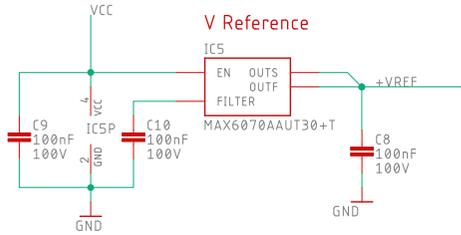


CLP-110-02-F-DH  
J2

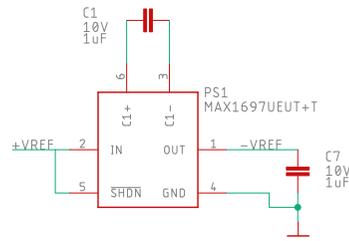


Optional I2C Resistors  
Do not Fit

# Power Supply



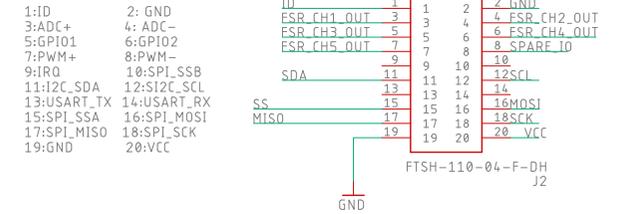
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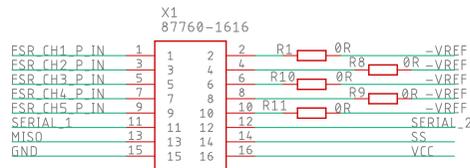
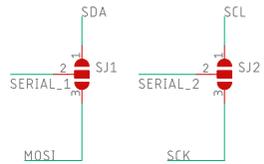
# Pressure Sensor SPI Header



# INPUT Header

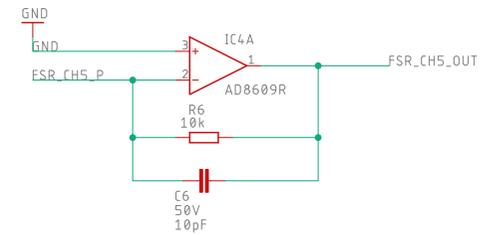
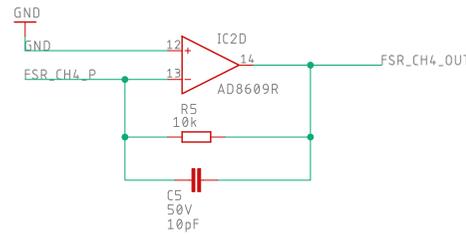
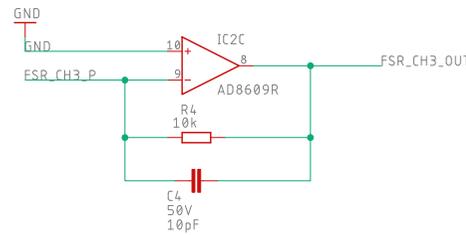
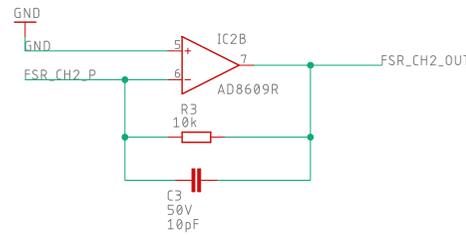
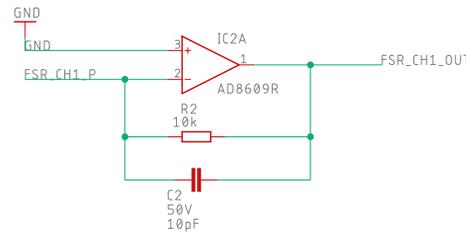
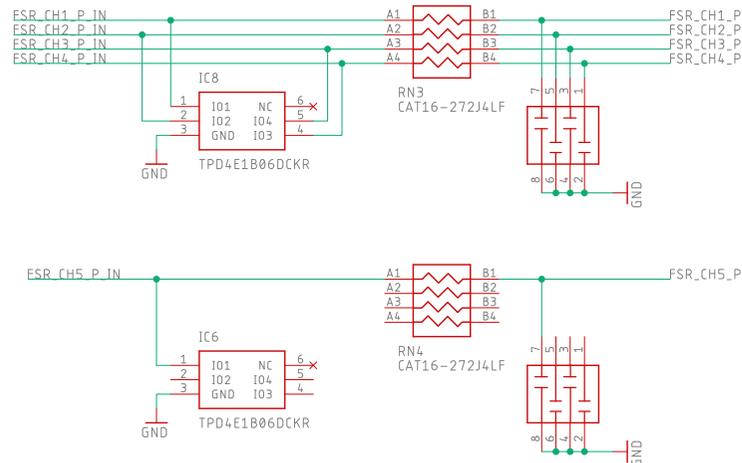


# Input Connector

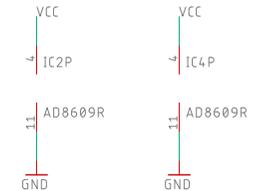


Do Not Place Resistors by default  
- install only top or bottom, Not Both

# Input Protection



# Opamp Power Rails



Alternate IC = TLV4333

TITLE: 2\_motor\_slave

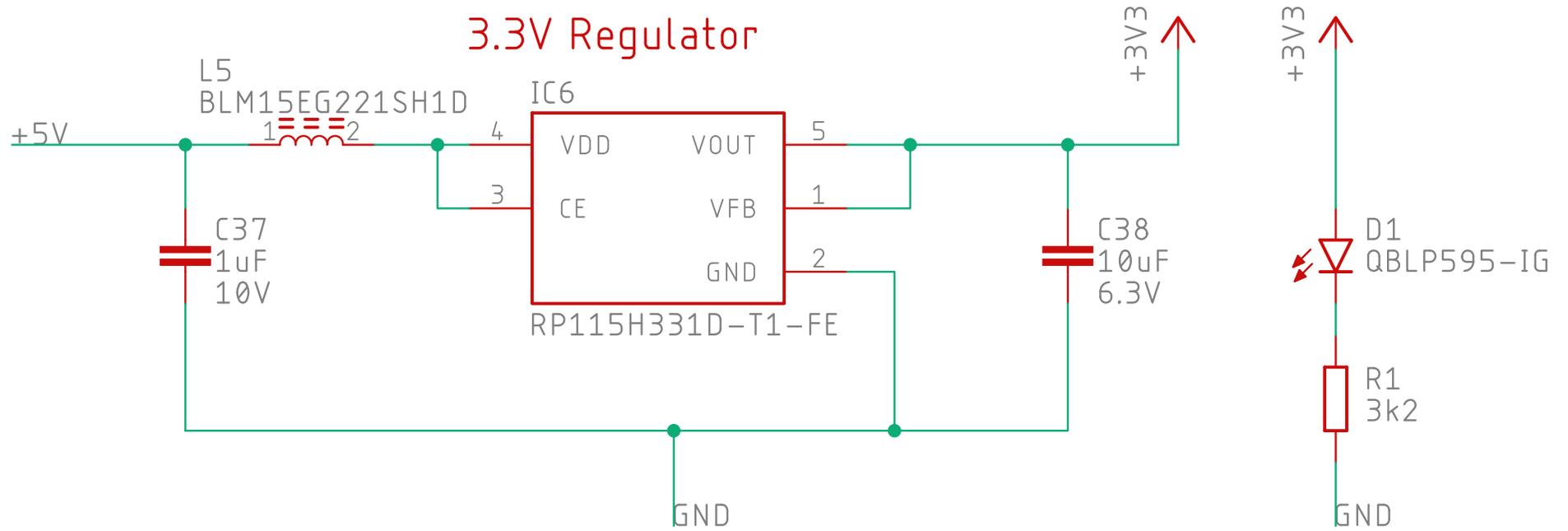
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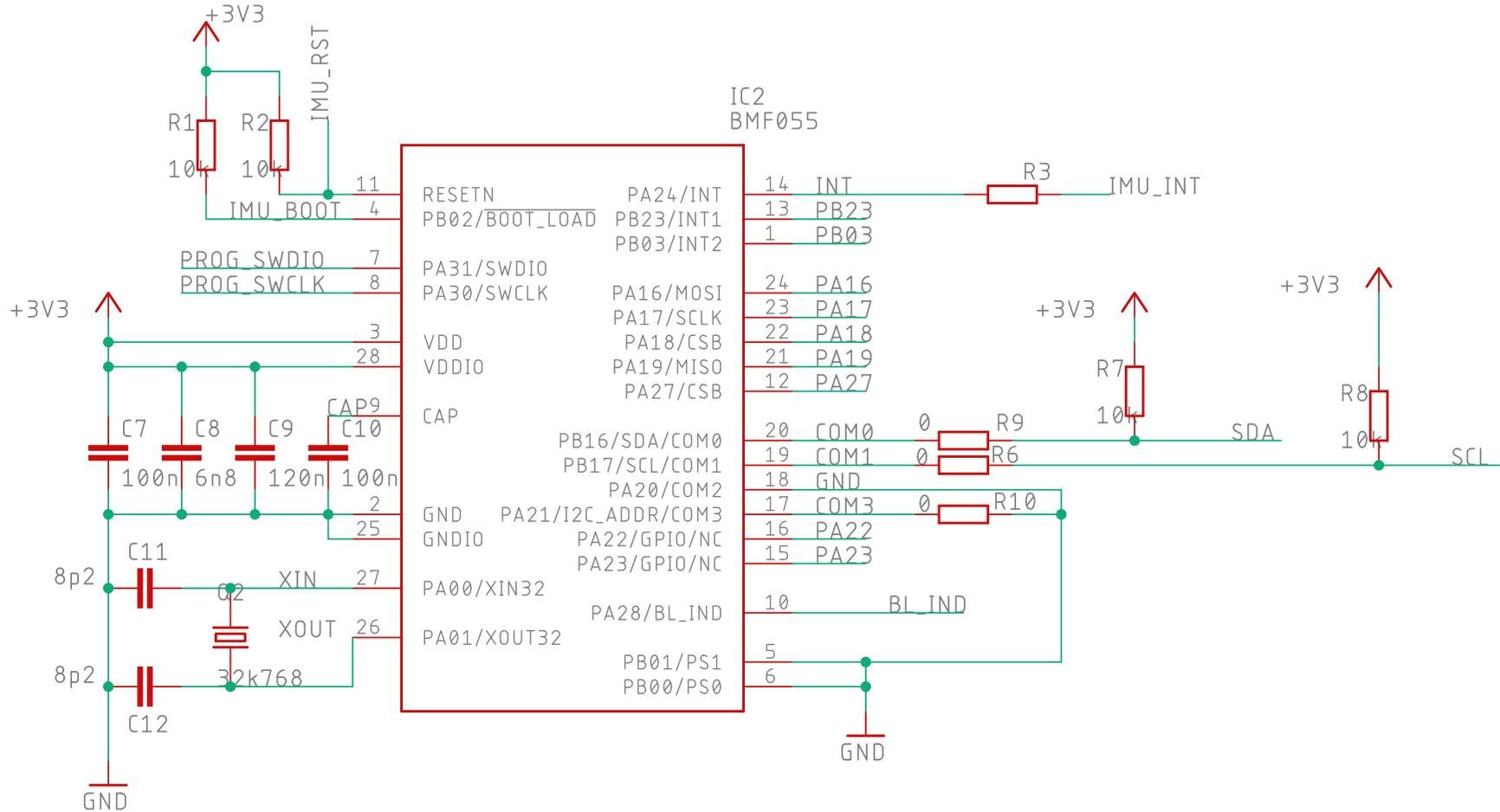
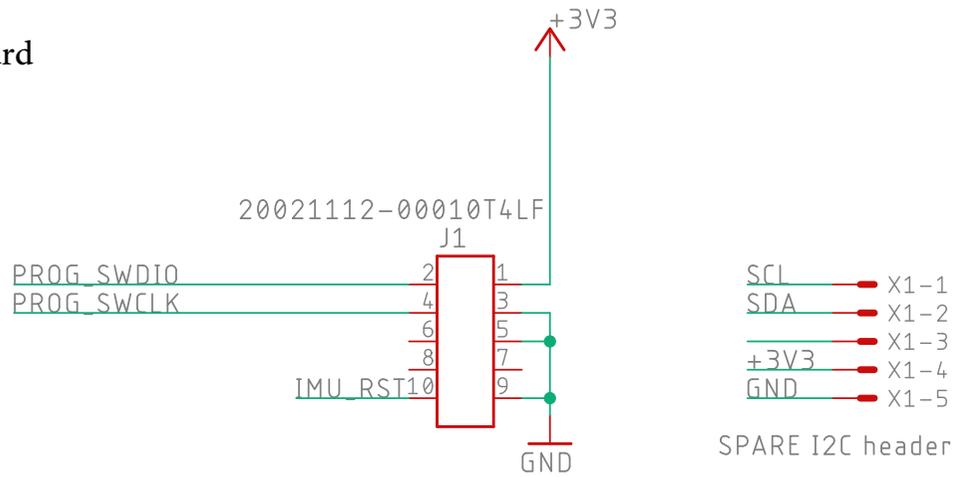
Date: 15/11/2021 18:53

Sheet: 1/1

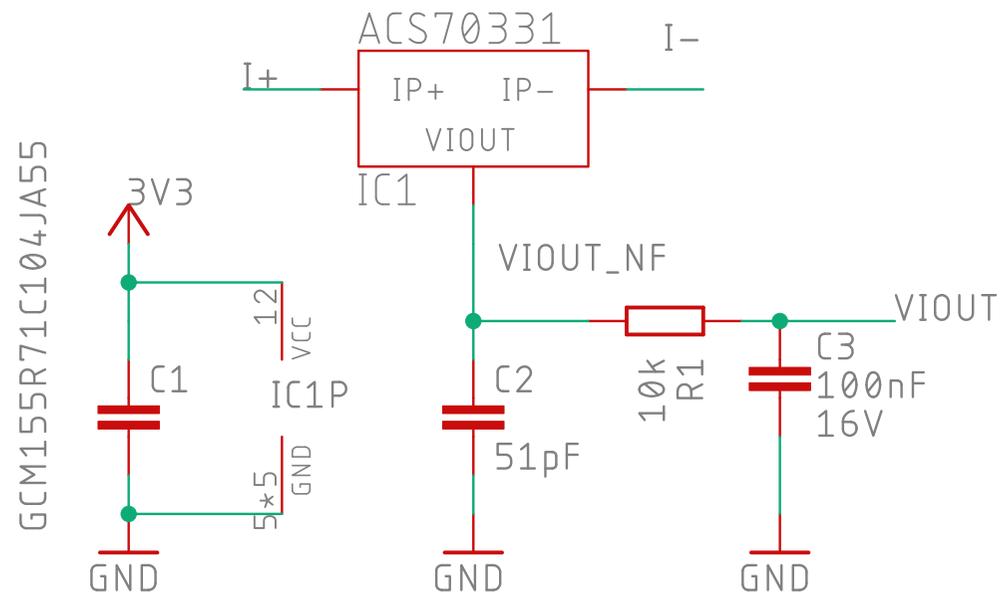
# Master Control Board



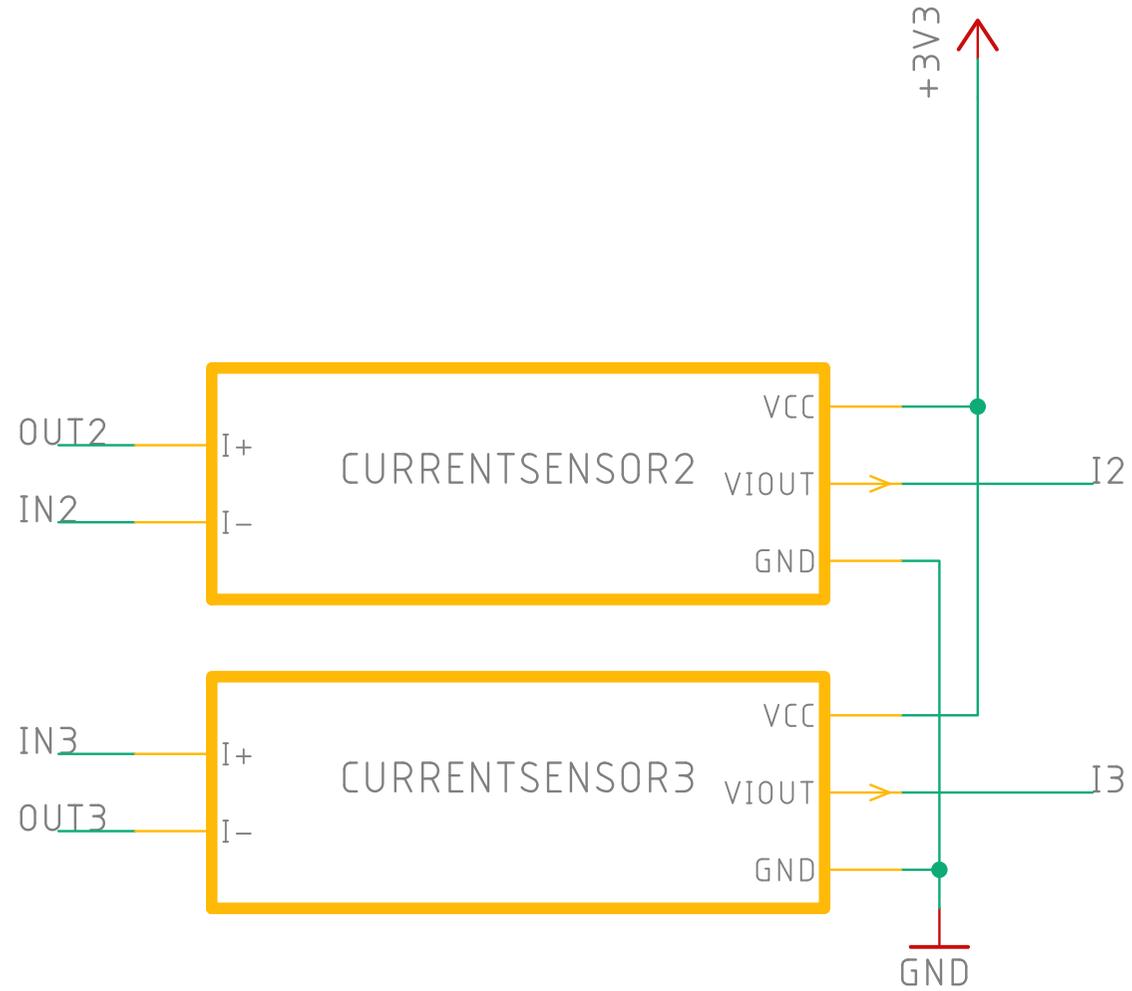
# Master Control Board



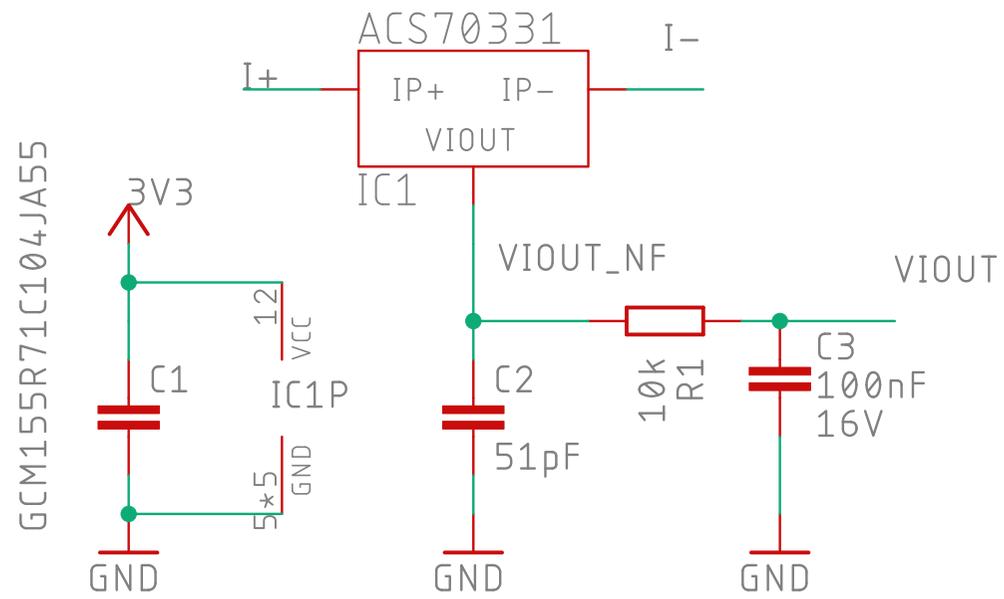
# Master Control Board



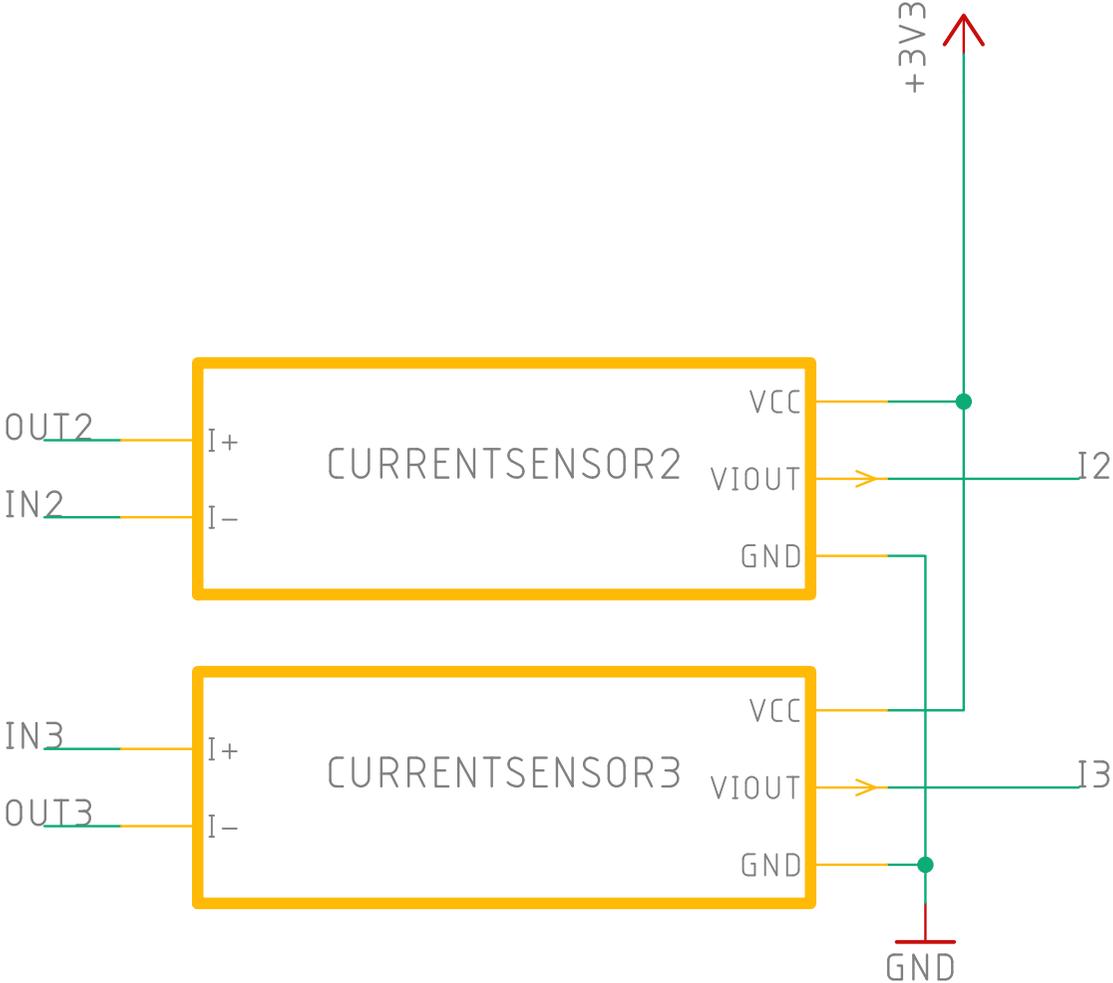
# Master Control Board



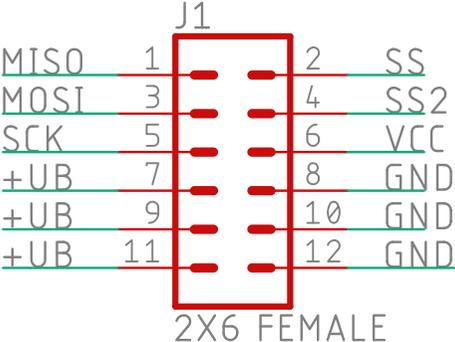
# Master Control Board



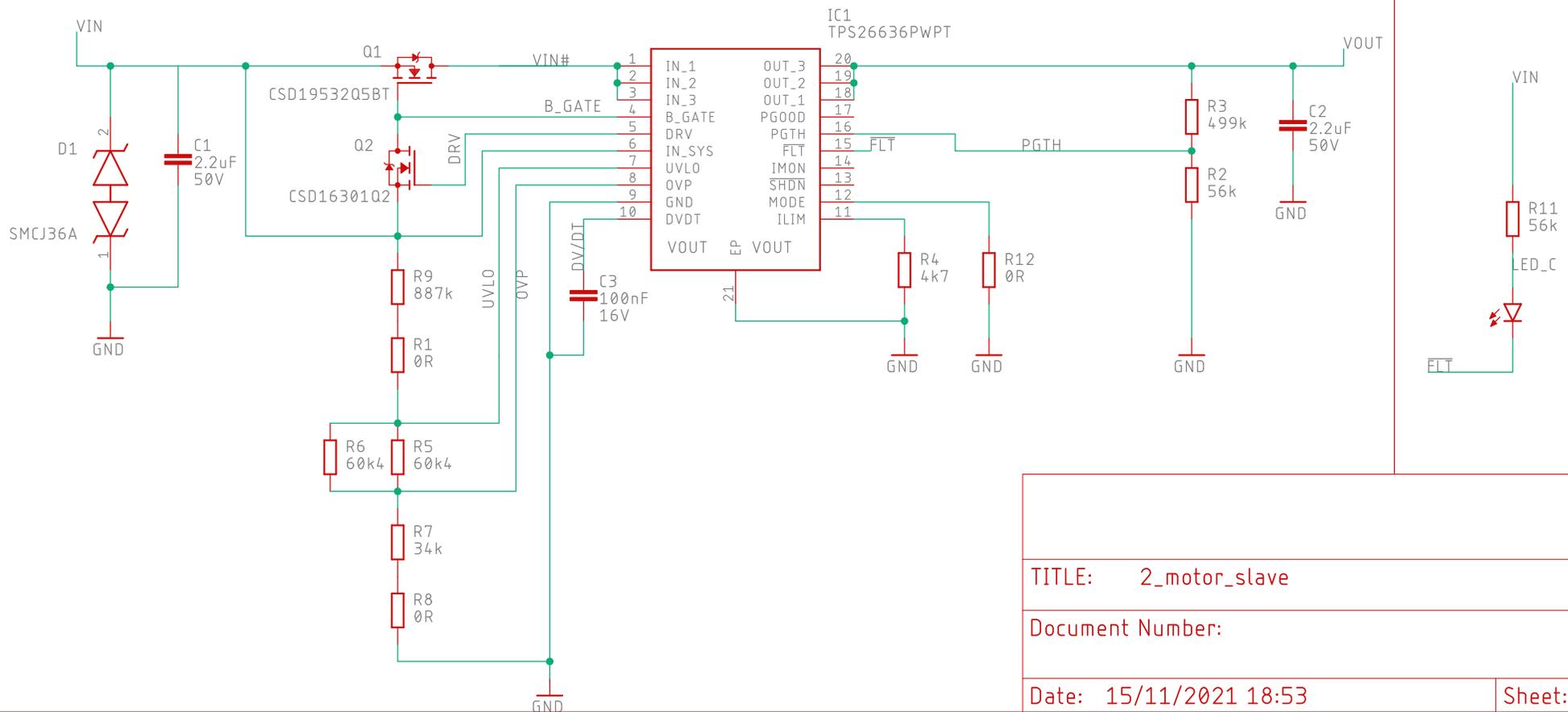
Master Control Board



Master Control Board



# Master Control Board



TITLE: 2\_motor\_slave

Document Number:

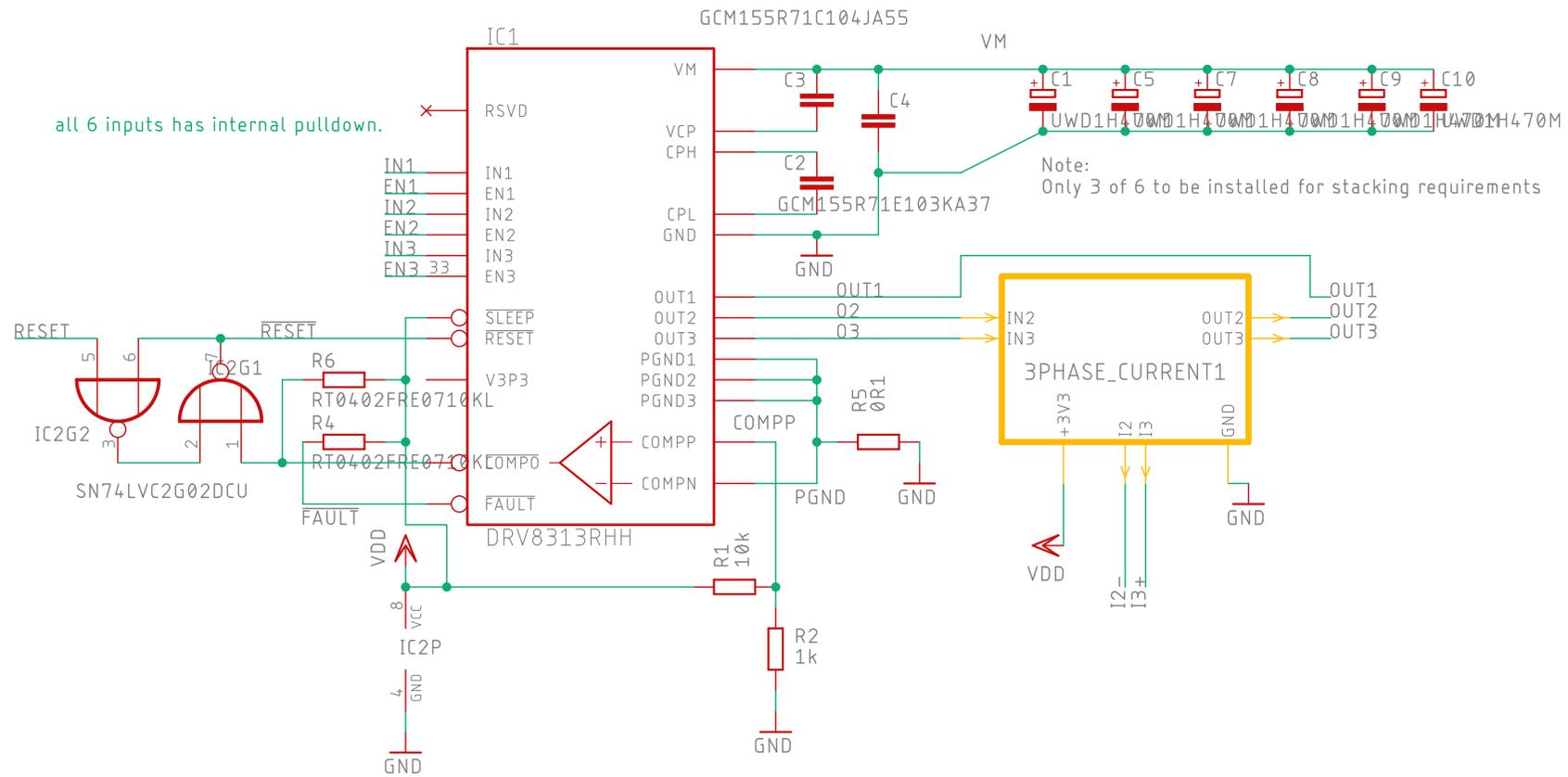
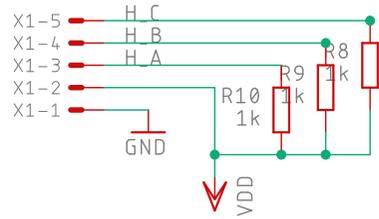
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Date: 15/11/2021 18:53

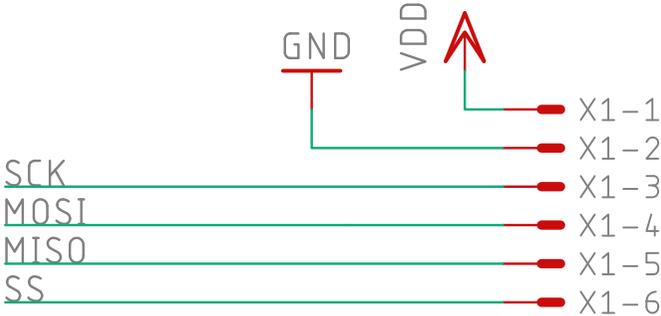
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# Master Control Board

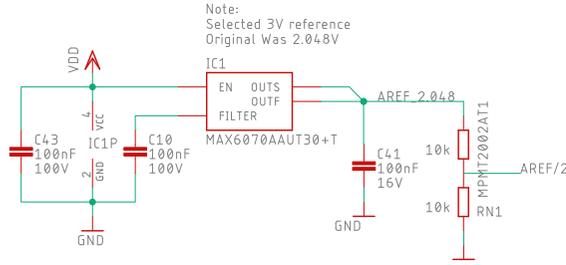


Master Control Board

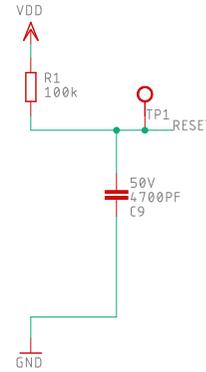


Daisy chaining done Offboard

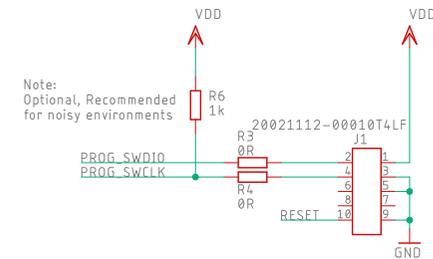
# ADC REF Master Control Board



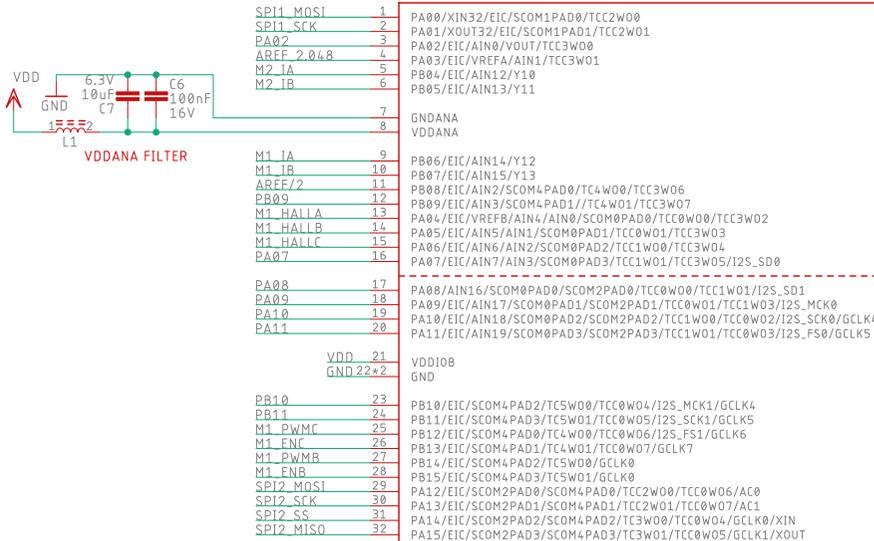
# RESET



# PROG HEADER



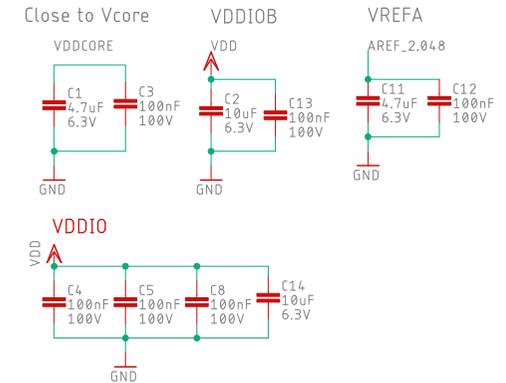
# U\$2 ATSAME51J19A-MUT



# TESTPOINTS



# DECOUPLING



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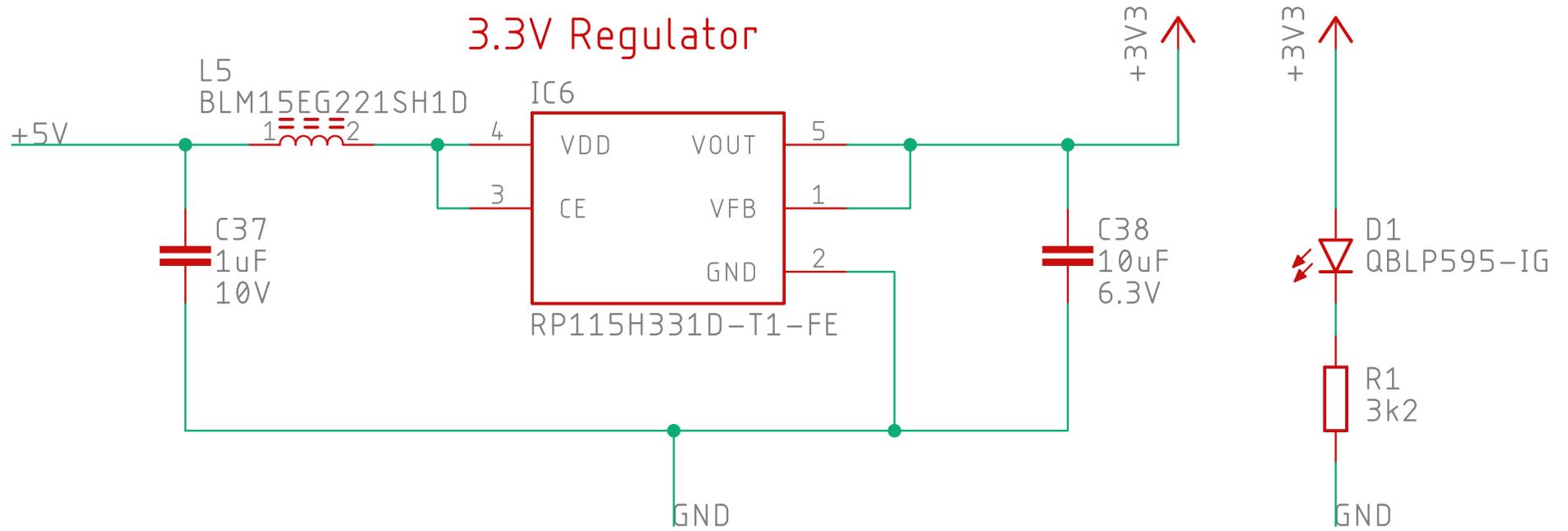
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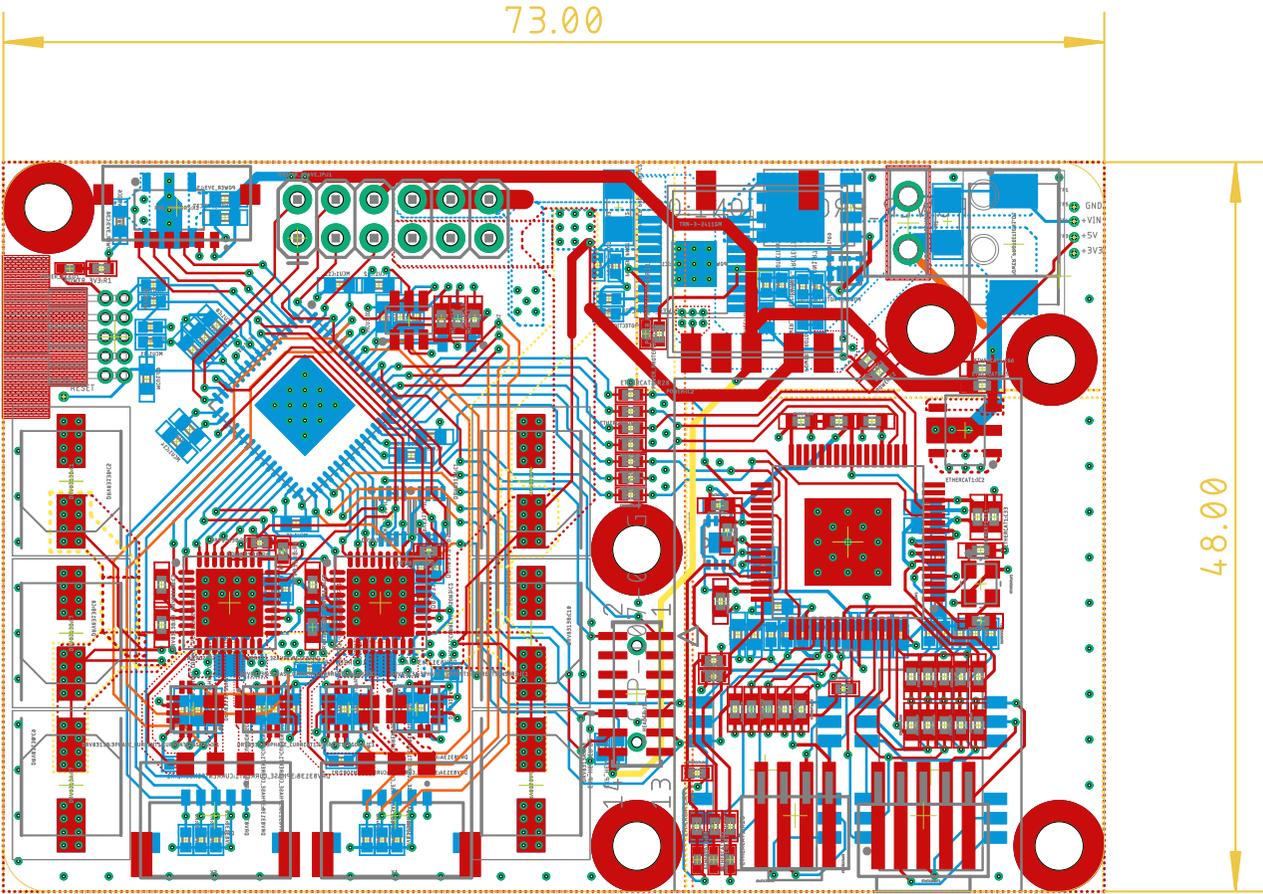
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Sheet: 1/1

# Master Control Board



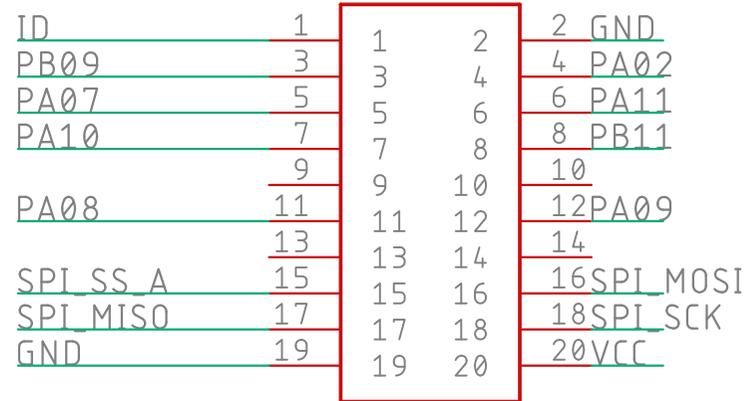
Master Control Board Layout





# Slave Control Board

1:ID	2: GND
3:ADC+	4: ADC-
5:GPIO1	6:GPIO2
7:PWM+	8:PWM-
9:IRQ	10:SPI_SSB
11:I2C_SDA	12:SI2C_SCL
13:USART_TX	14:USART_RX
15:SPI_SSA	16:SPI_MOSI
17:SPI_MISO	18:SPI_SCK
19:GND	20:VCC

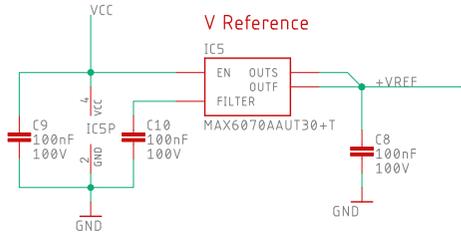


CLP-110-02-F-DH  
J2

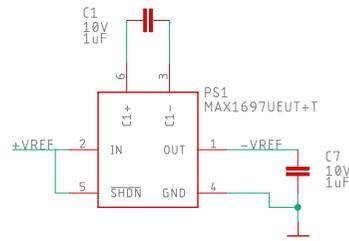


Optional I2C Resistors  
Do not Fit

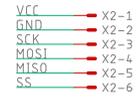
# Power Supply



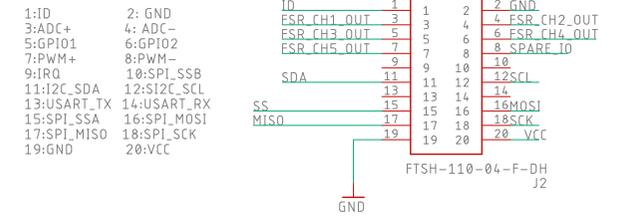
# Voltage Inverter



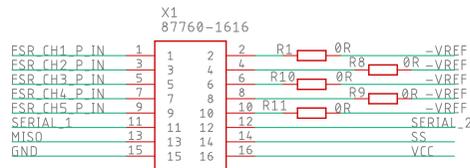
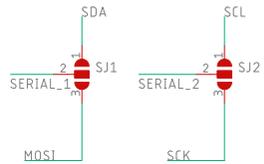
# Pressure Sensor SPI Header



# INPUT Header

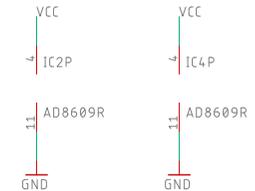


# Input Connector

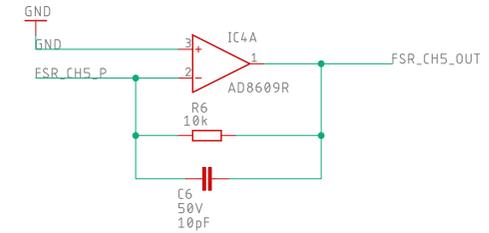
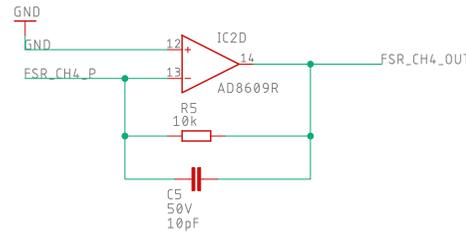
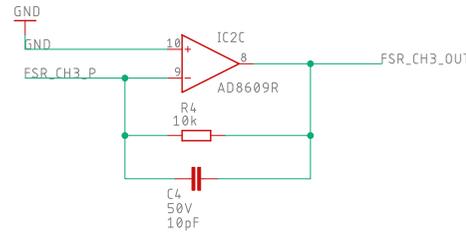
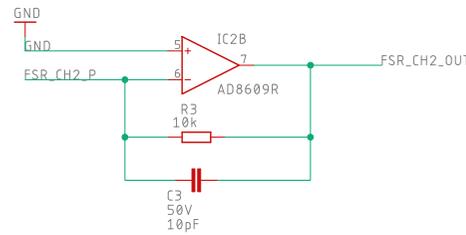
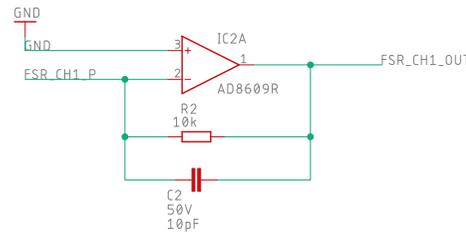
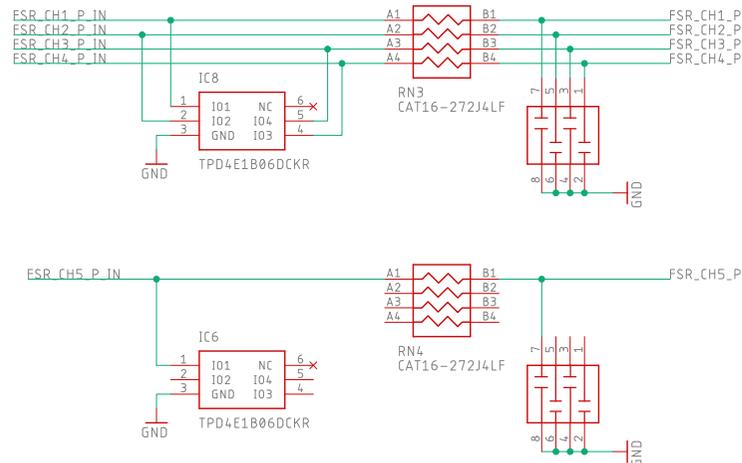


Do Not Place Resistors by default  
- install only top or bottom, Not Both

# Opamp Power Rails



# Input Protection



Alternate IC = TLV4333

TITLE: 2\_motor\_slave

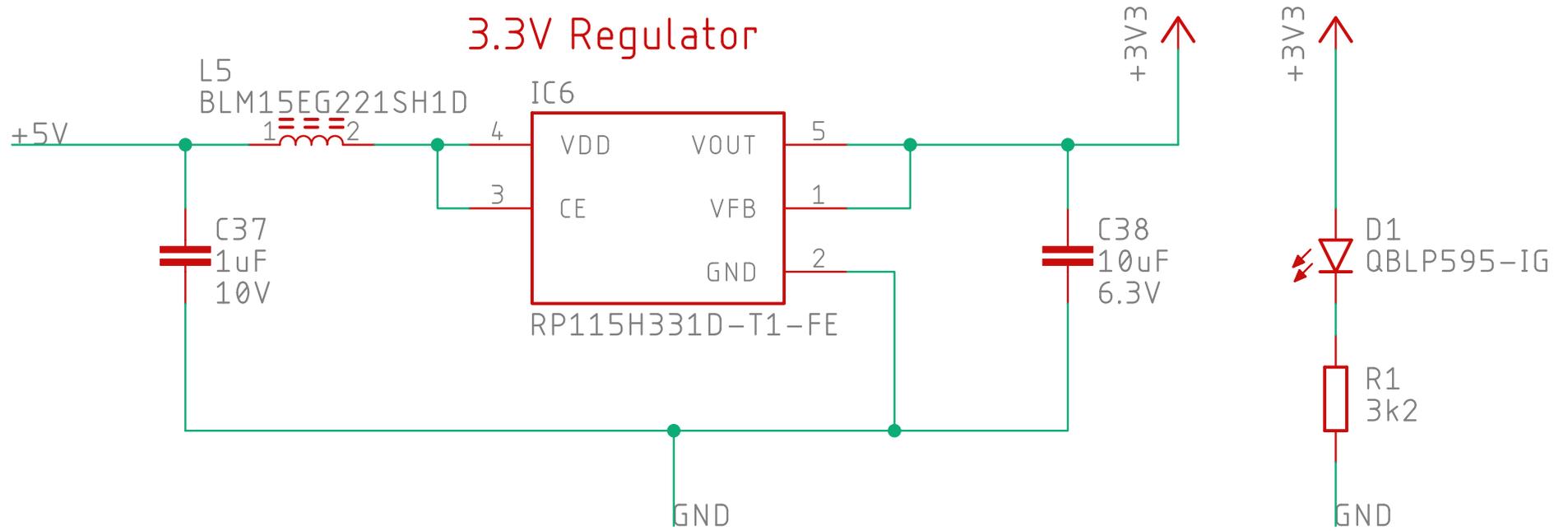
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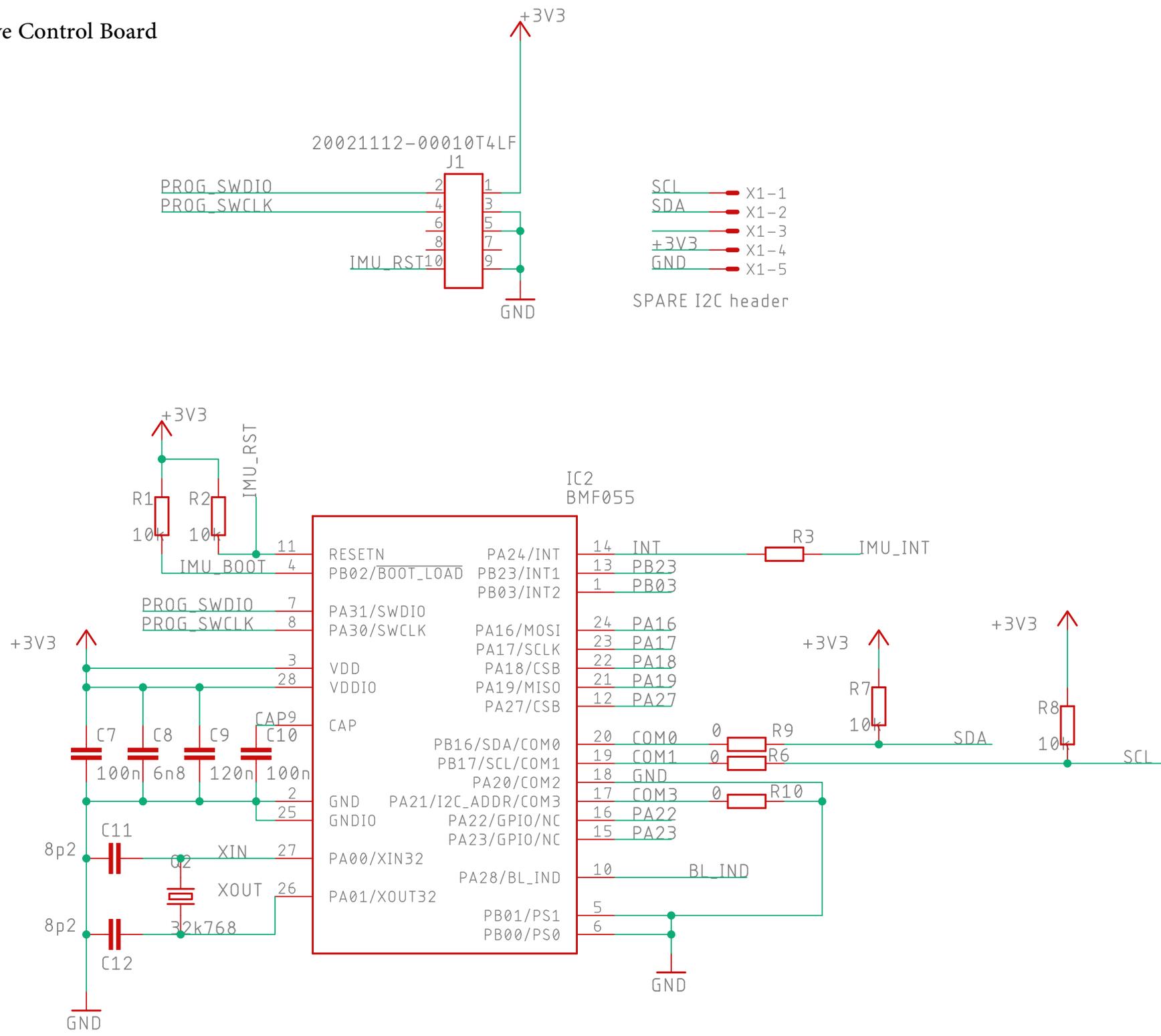
Date: 15/11/2021 18:53

Sheet: 1/1

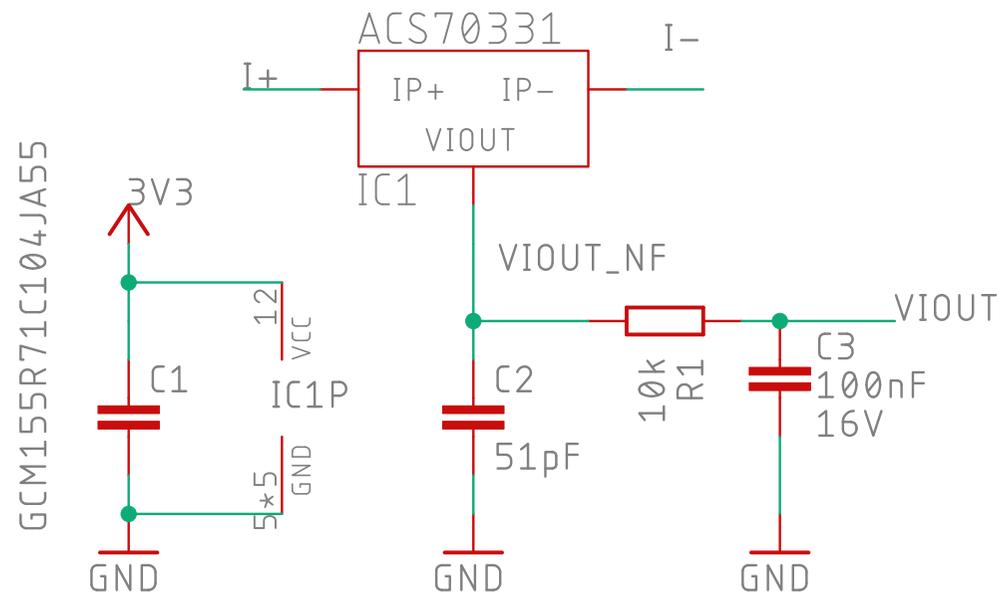
# Slave Control Board



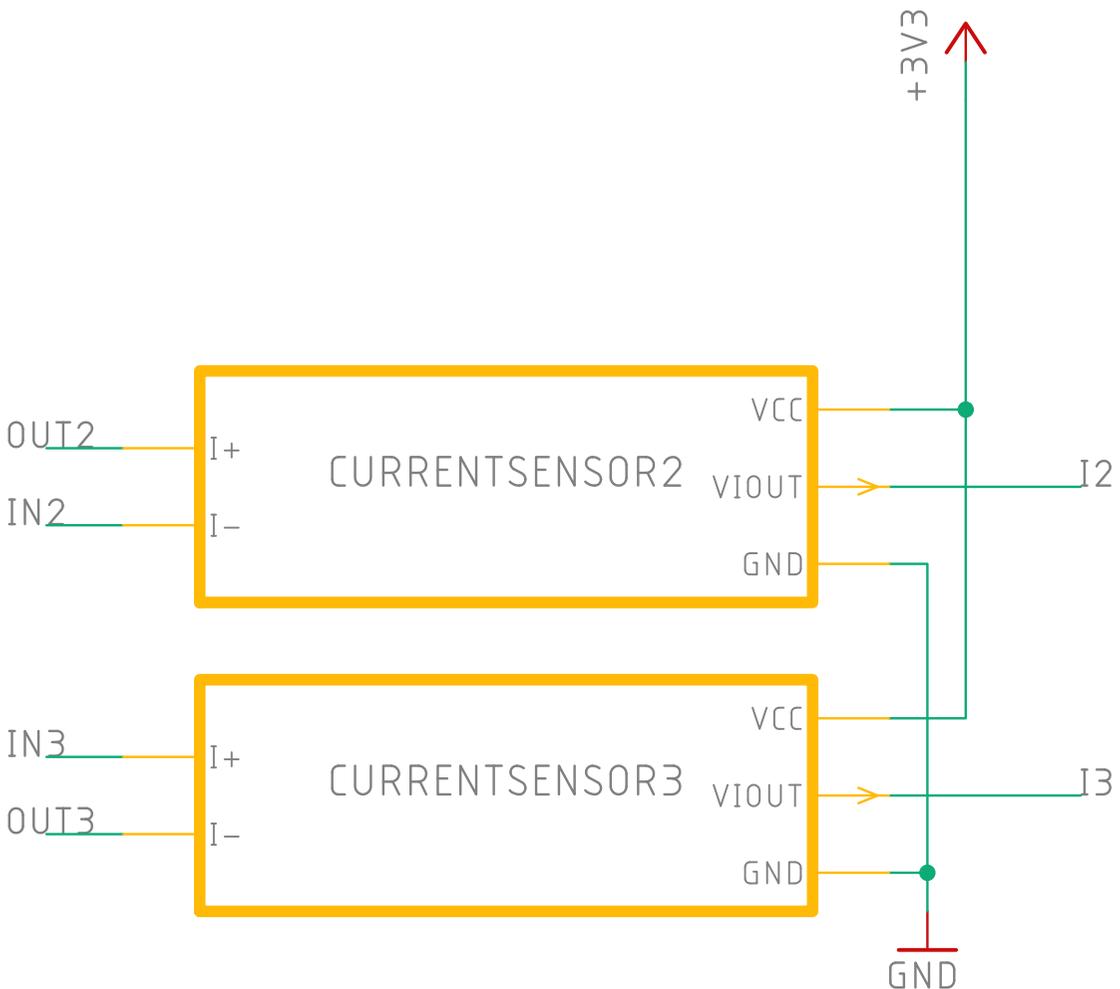
# Slave Control Board



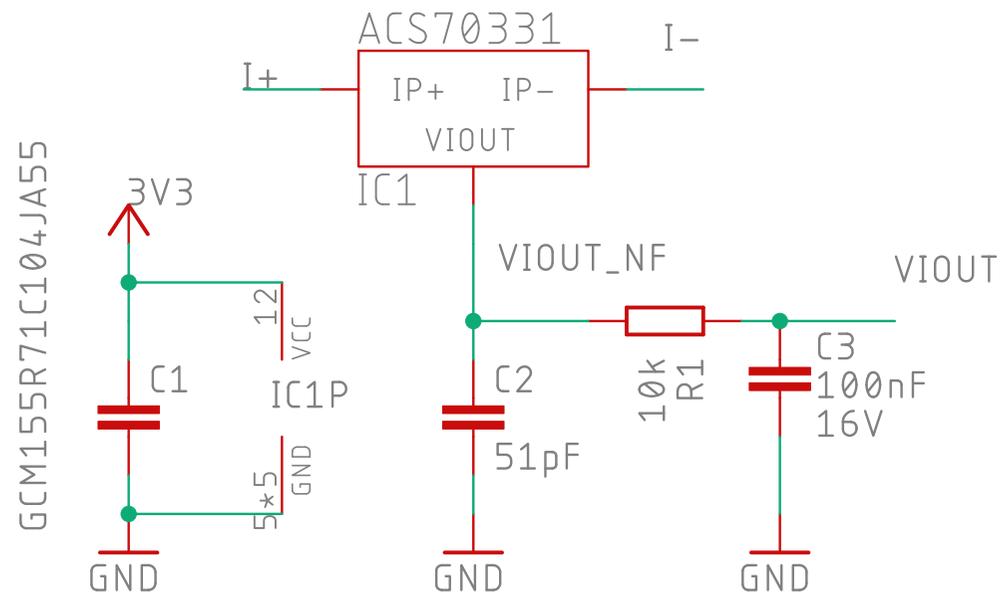
# Slave Control Board



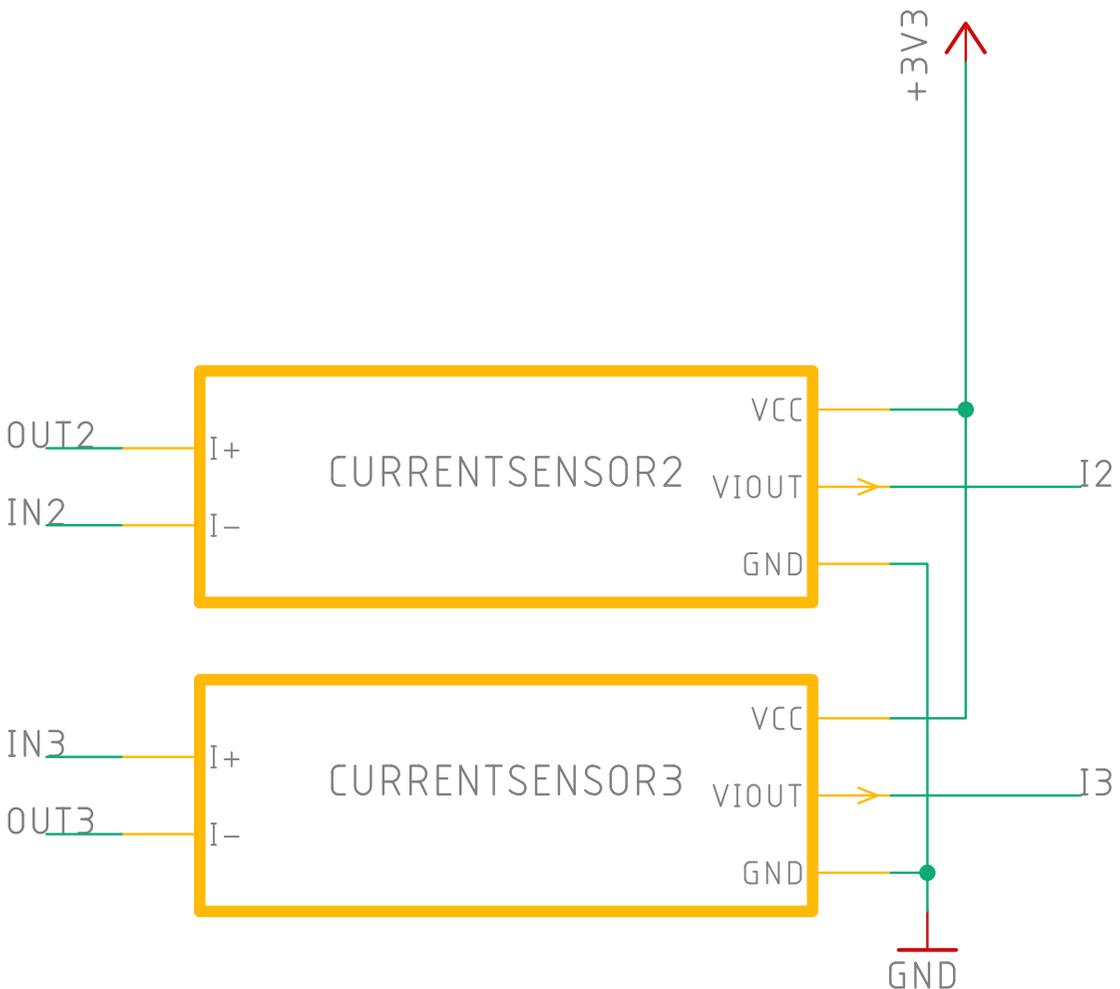
Slave Control Board



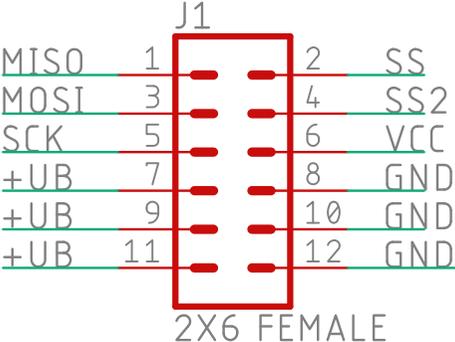
# Slave Control Board



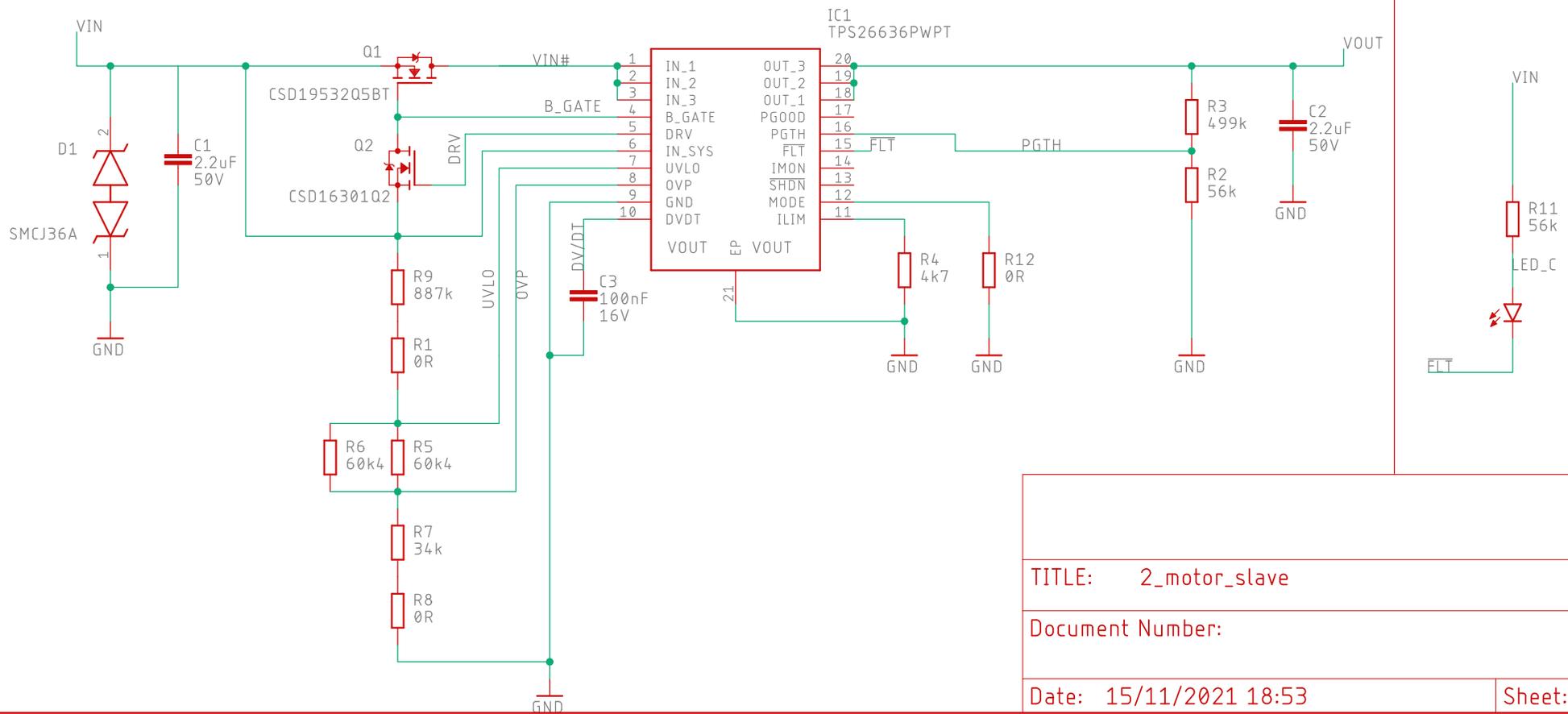
Slave Control Board



Slave Control Board

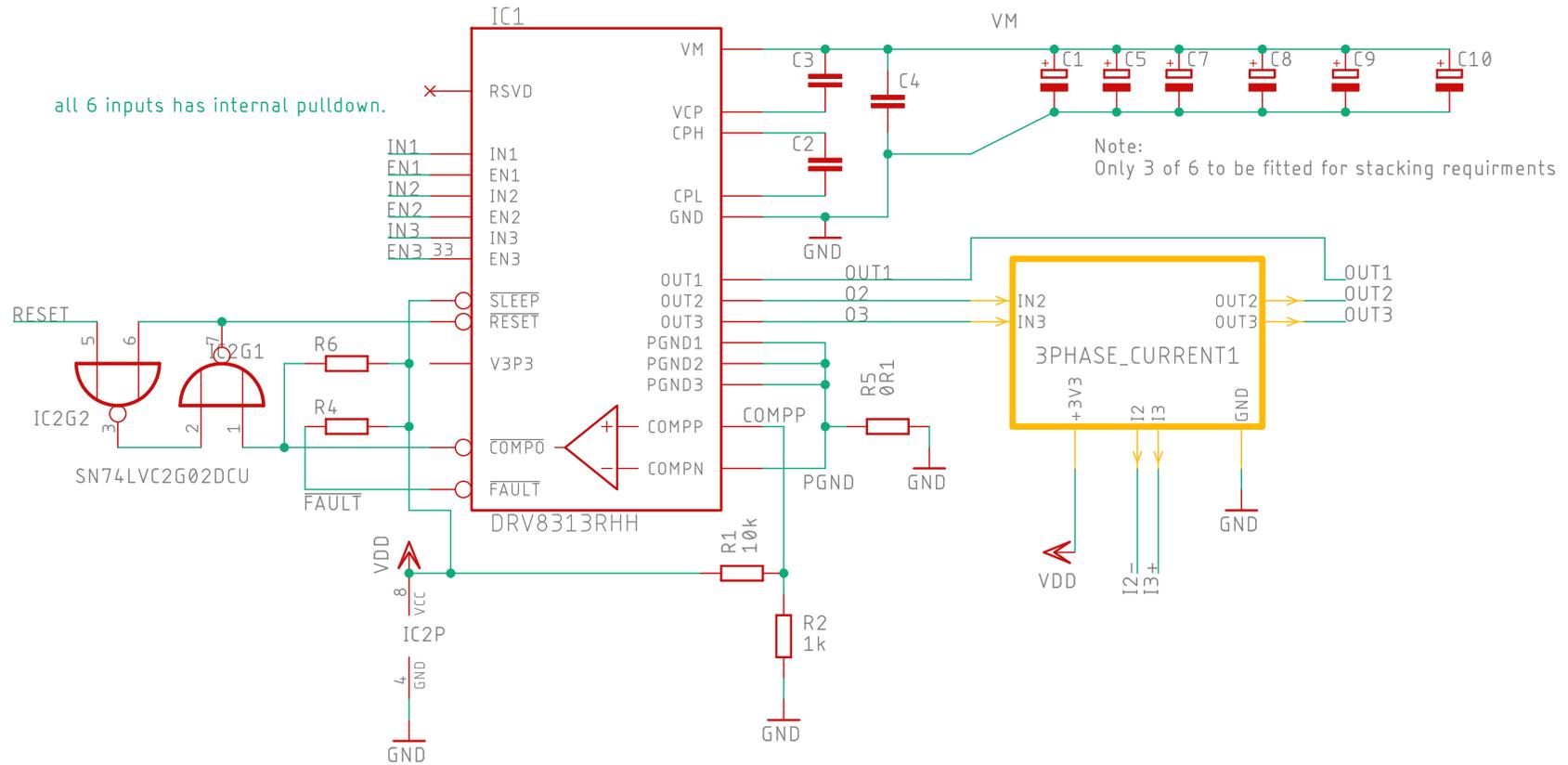
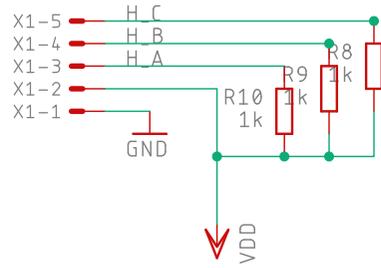


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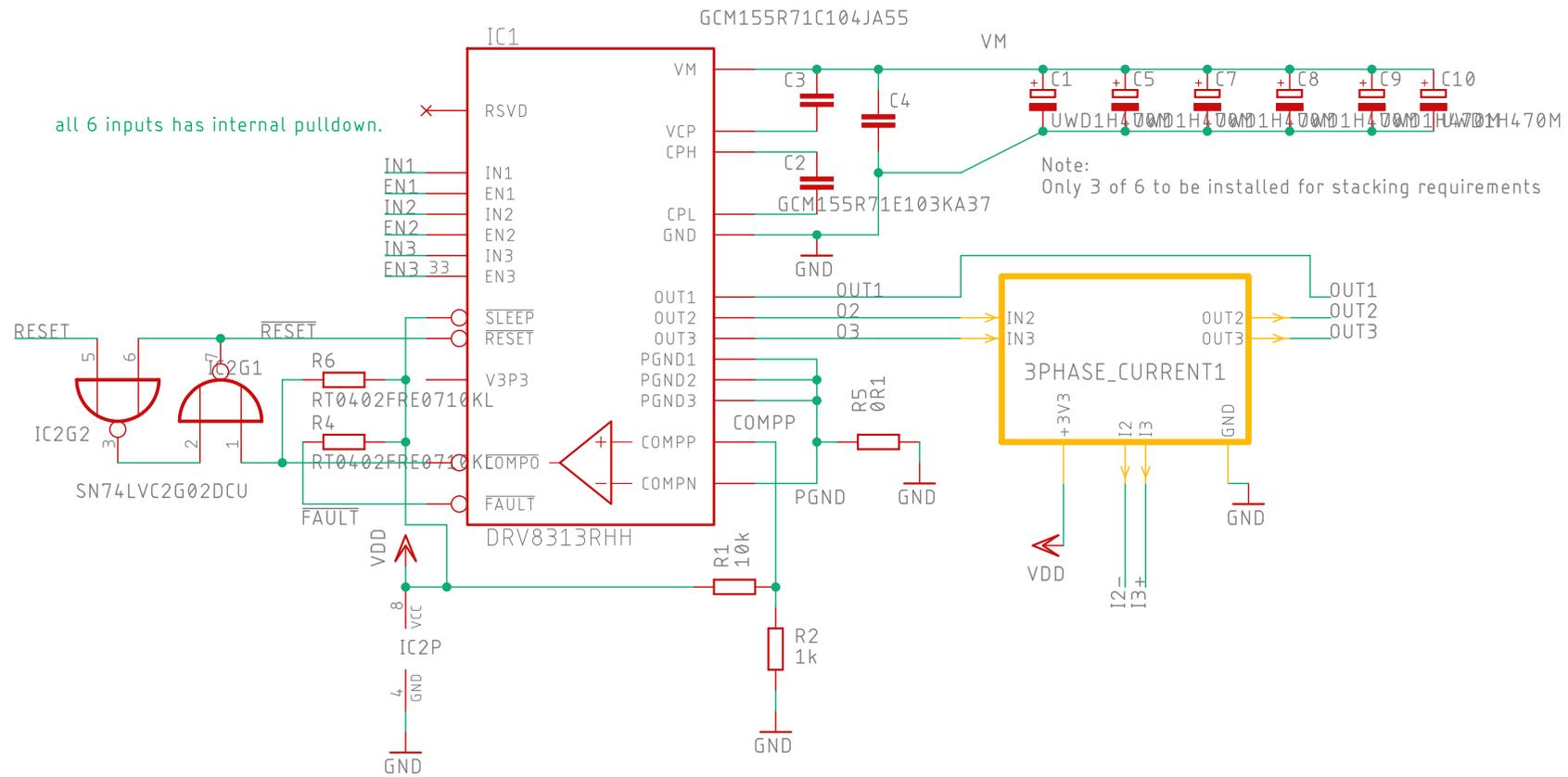
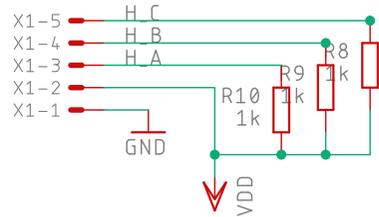


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Document Number:	REV:
Date: 15/11/2021 18:53	Sheet: 1/1

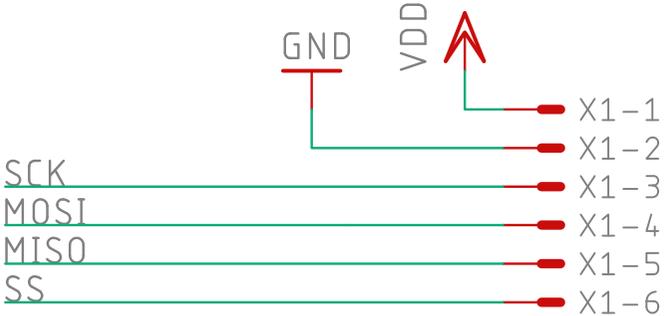
# Slave Control Board



# Slave Control Board

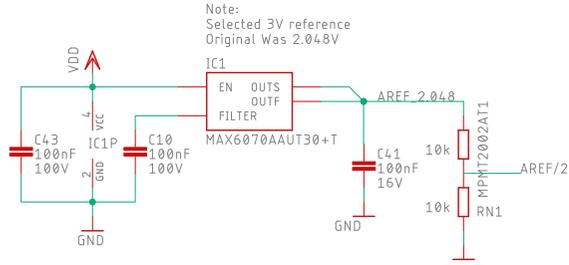


Slave Control Board

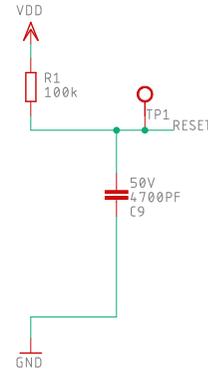


Daisy chaining done Offboard

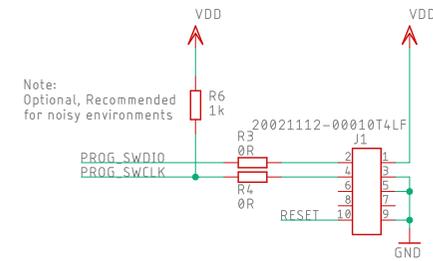
# ADC REF Slave Control Board



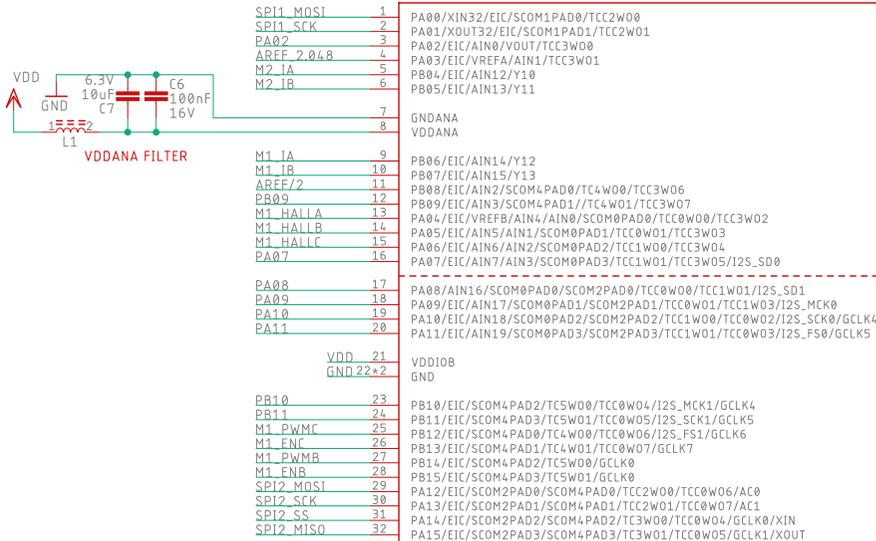
# RESET



# PROG HEADER



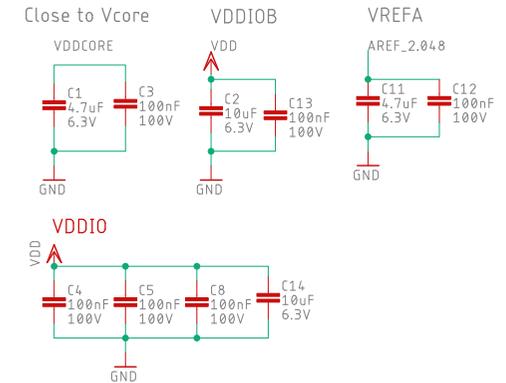
## U\$2 ATSAME51J19A-MUT



# TESTPOINTS



# DECOUPLING



TITLE: 2\_motor\_slave

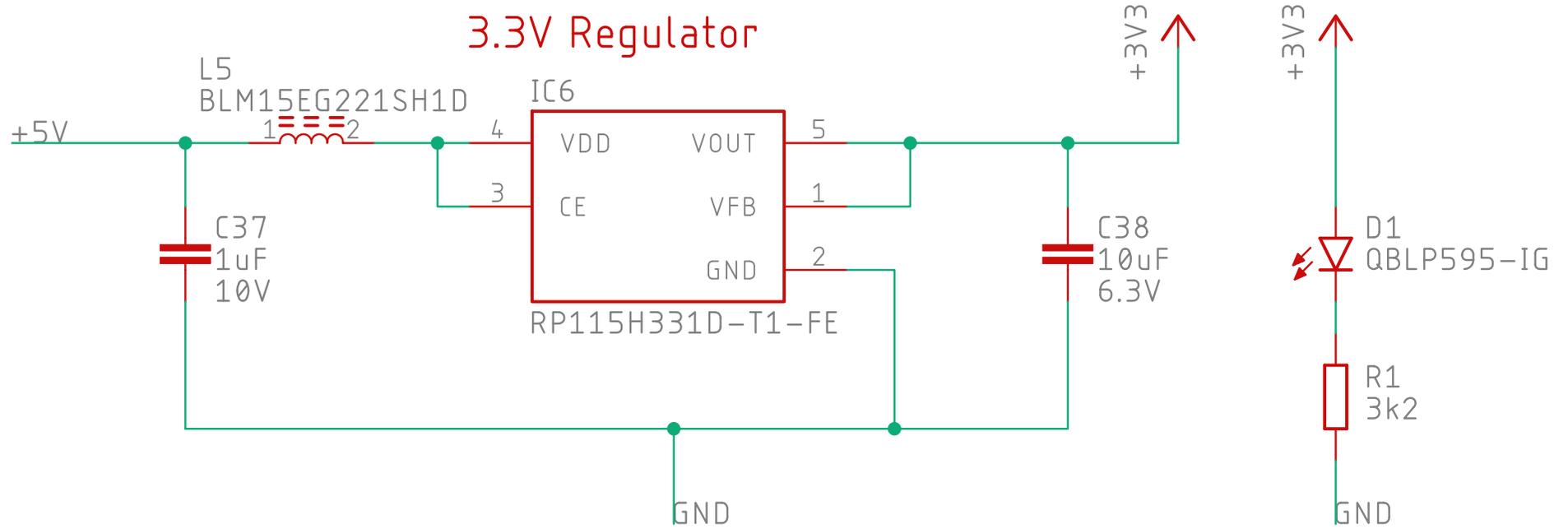
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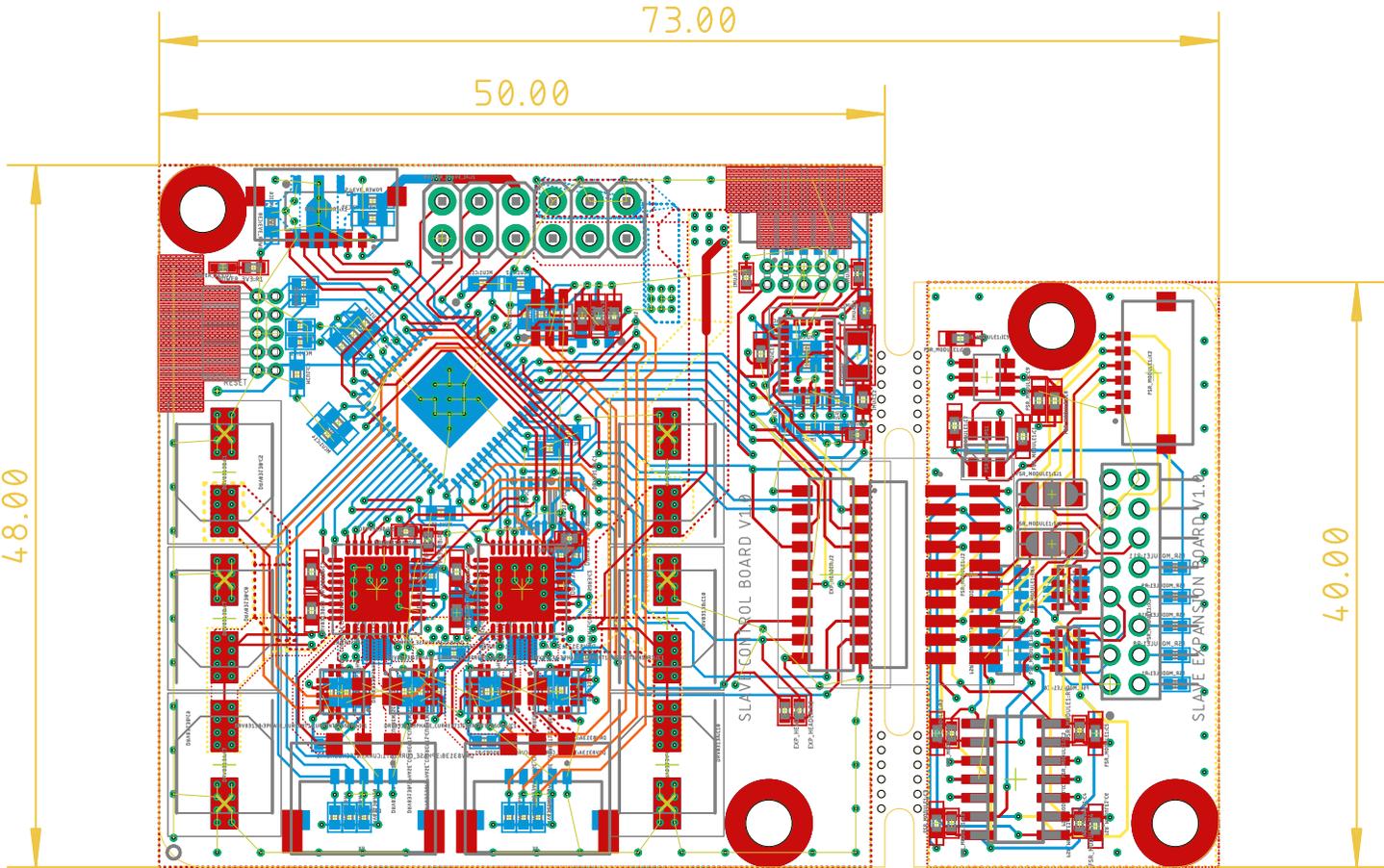
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Sheet: 1/1

# Slave Control Board

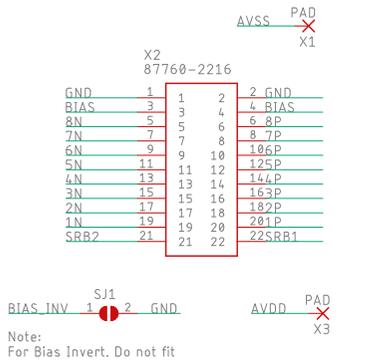


# Slave Control Board Layout

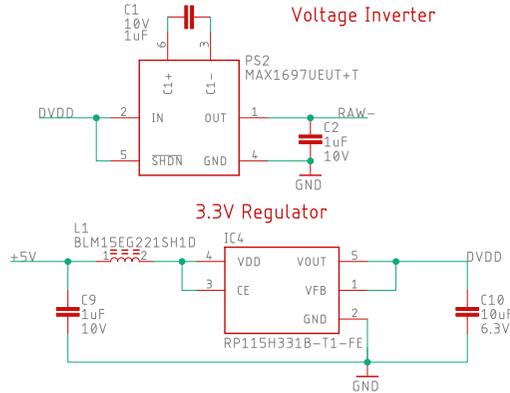


# EMG Board

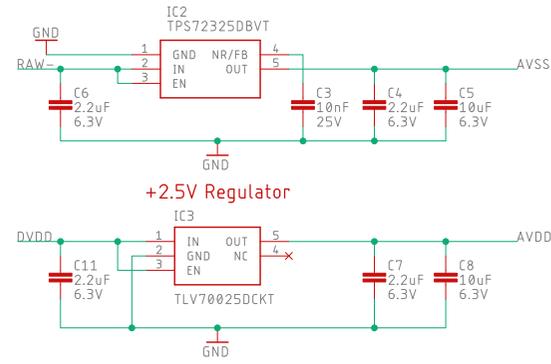
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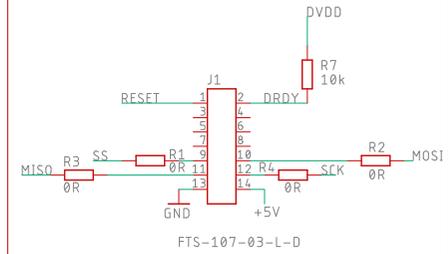
## Power Supply



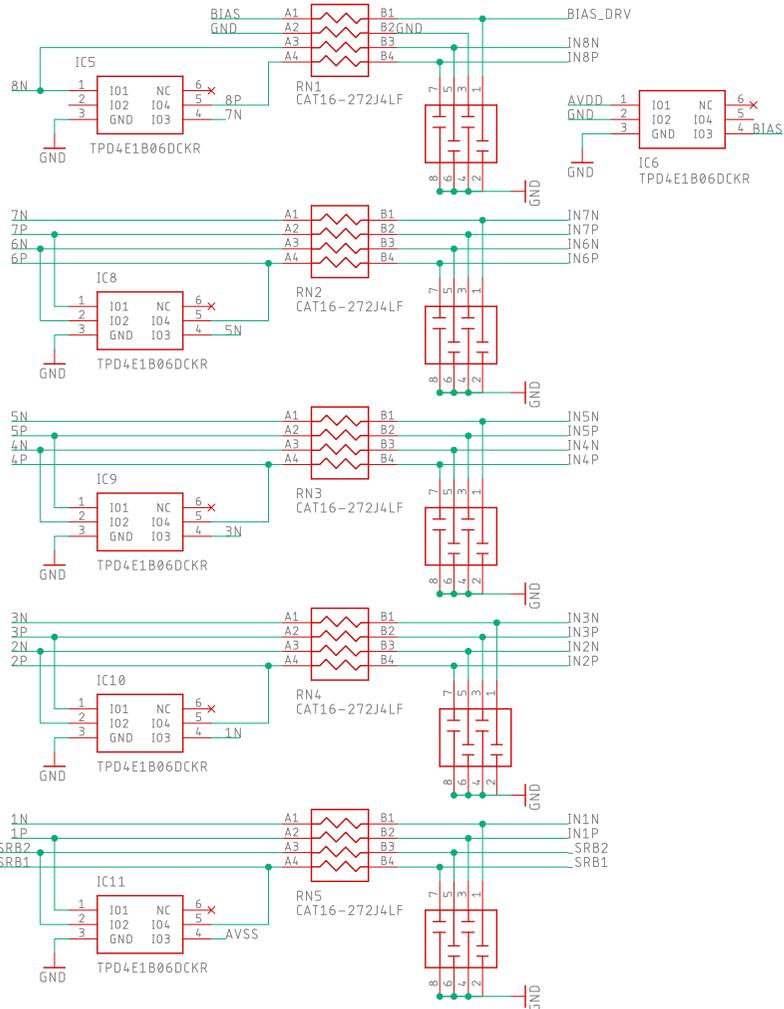
## -2.5V Regulator



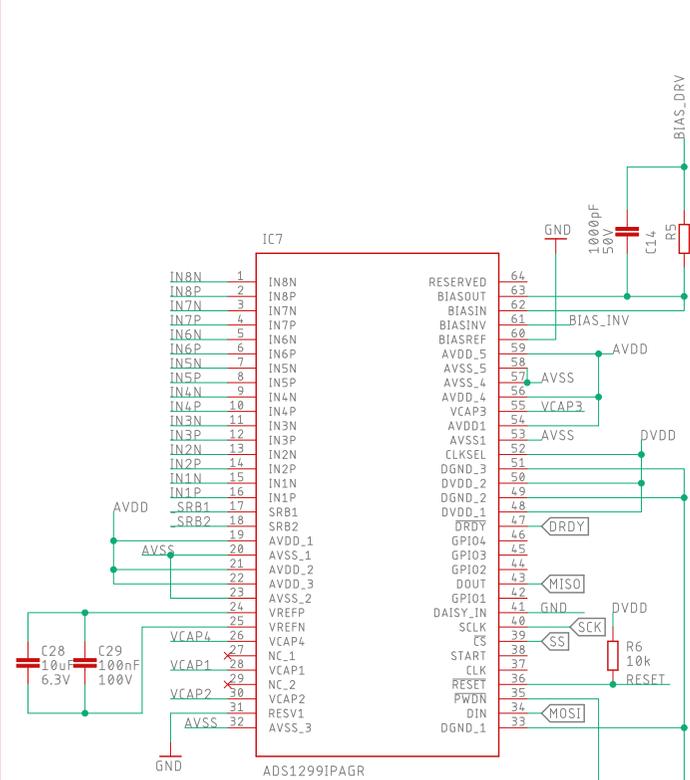
## Interface Connector



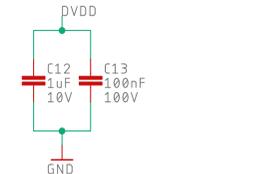
## Input Protection and Filtering



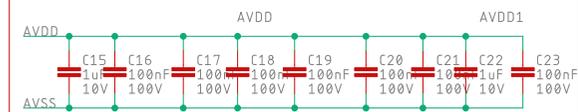
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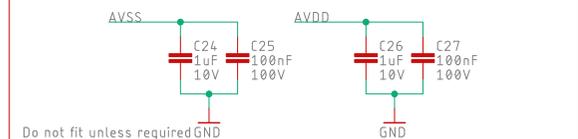
## DVDD DECOUPLING



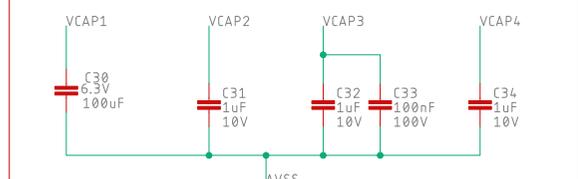
## AVDD DECOUPLING



## AVSS & VDD to GND



## VCAP



## EMG Interface ADS1299 Analog Front End

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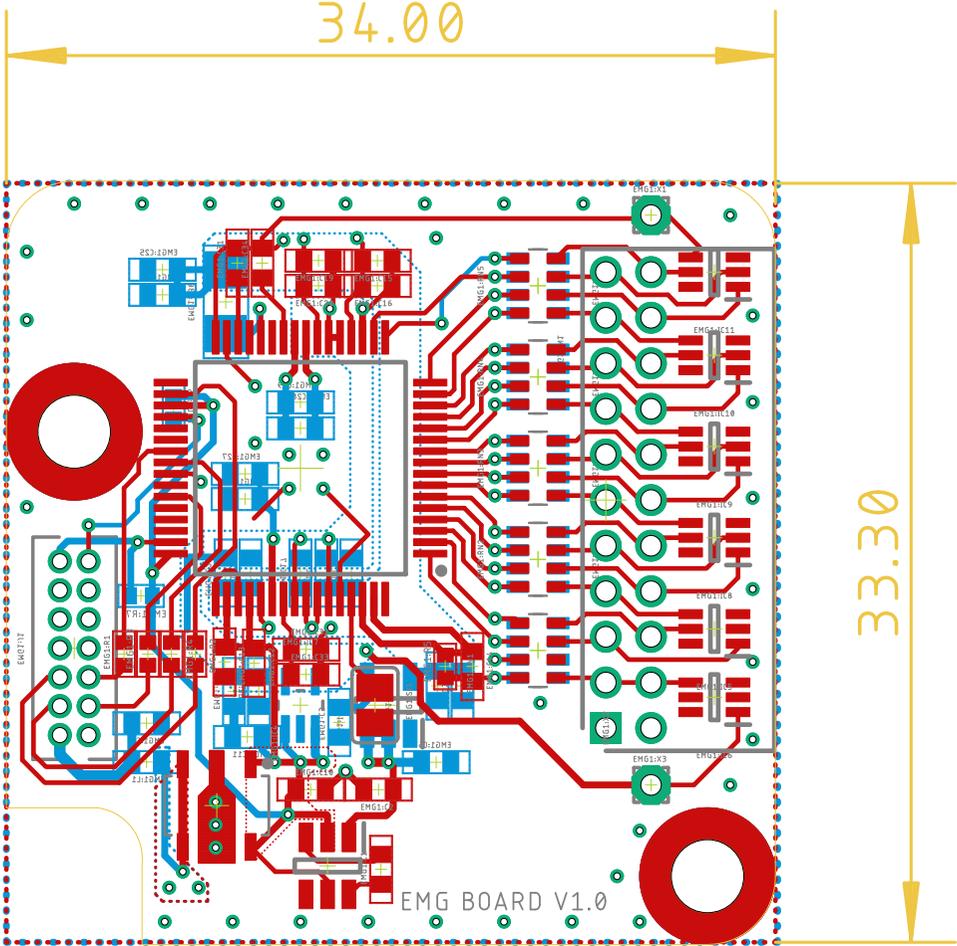
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Sheet: 1/1

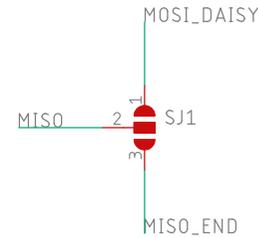
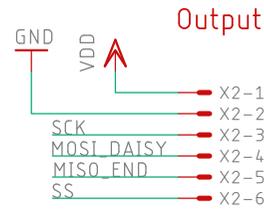
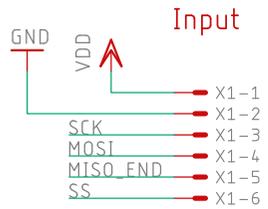
EMG Board Layout



EMG1P52

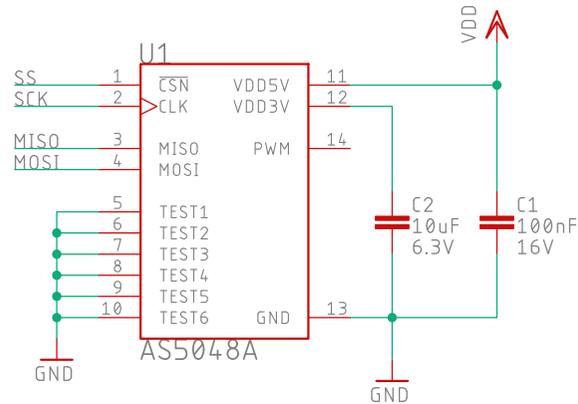
# Connectors

## AS5048 Angle Sensor



Note:

Daisy Chain Configuration, arbitrary number of slaves can be used but number needs to be hardcoded. Slaves in the middle of the chain need to set the jumper to "MOSI\_DAISY". Last slave in the chain needs to set the jumper to "MISO\_END" Position



TITLE: Angle\_Sensor\_AS5048\_picolock

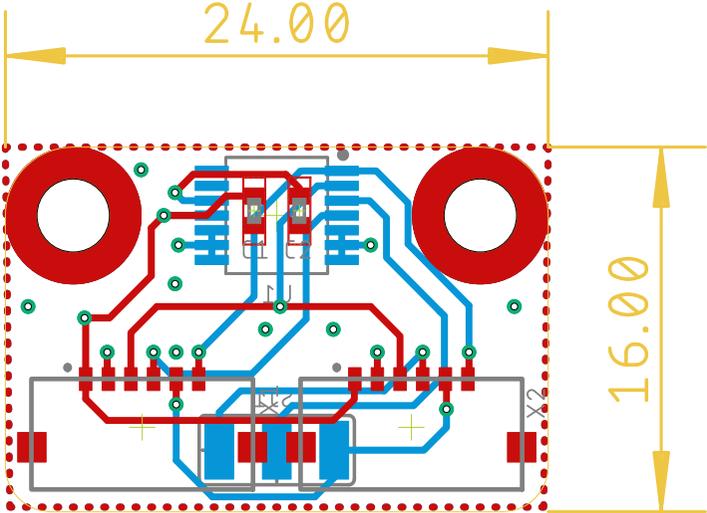
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Date: 03/07/2021 13:13

Sheet: 1/1

AS5048 Angle Sensor Layout

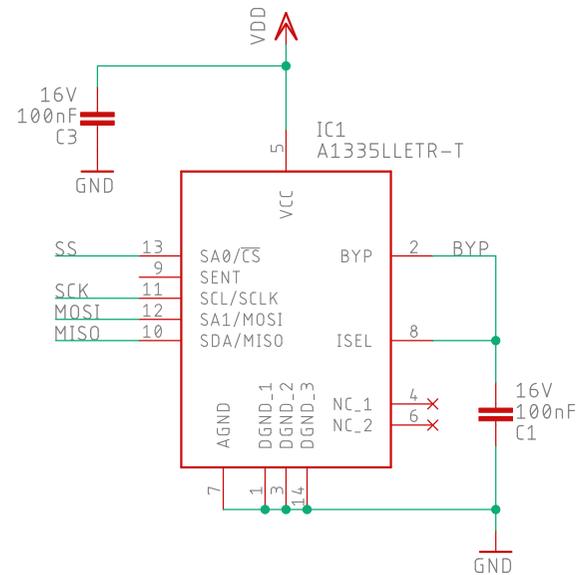
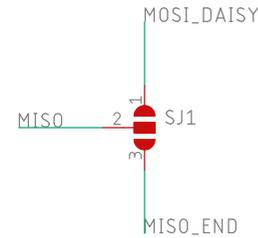
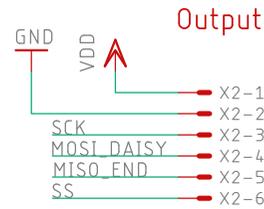
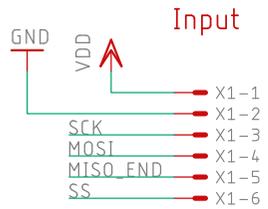


# Connectors

## A1335 Angle Sensor

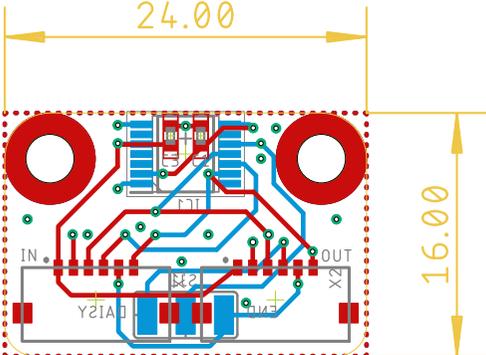
Note:

Daisy Chain Configuration, arbitrary number of slaves can be used but number needs to be hardcoded. Slaves in the middle of the chain need to set the jumper to "MOSI\_DAISSY". Last slave in the chain needs to set the jumper to "MISO\_END" Position



TITLE: Angle_Sensor_A1335_picolock	
Document Number:	REV:
Date: 01/07/2021 00:41	Sheet: 1/1

A1335 Angle Sensor



# C. Hardware Configuration Details and Calculations

## C.1. TPS26636

The typical application circuit used to implement the required safety features are shown in [Figure C.1](#) for clarity.

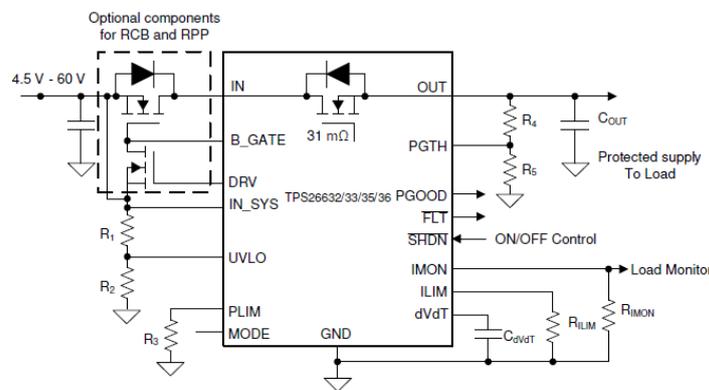


Figure C.1.: TPS26635 Application Circuit [Tps]

The protection features provided by the eFuse include:

- [Reverse Polarity Protection \(RPP\)](#) & [Reverse Current Blocking \(RCB\)](#)
- [Active over current Limiting](#) & [In-rush current limiting](#) ( $\frac{dv}{dt}$ )
- [Over Voltage Protection \(OVP\)](#) and surge suppression
- [Fast Short Circuit Protection \(SCP\)](#)
- [Under-Voltage Lock Out \(UVLO\)](#) set to a typical battery voltage cutout point

A summary of the desired design parameters and resulting calculated component values are shown in [Table C.1](#). The desired operating characteristics are listed as design inputs section. Resistor and capacitor values were then selected to configure the device using the equations provided in the device datasheet [Tps]. The selected UVLO value is based on a 6S battery pack which should not be discharged below 3.6V per cell. The results of the design calculations are shown in the results section.

Design Inputs	Description	Value	Units
$V_{in(min)}$	Minimum Operating Input Voltage	21.5	V
$V_{in(max)}$	Maximum Operating Input Voltage	33.0	V
$V_{in(nom)}$	Nominal Input Voltage	24.0	V
$UV_{set}$	Under-voltage Lockout Set point	21.6	V
$I_{max}$	Maximum continuous load current	4.5	A
$I_{inrush(max)}$	Permissible inrush current on Start-up	1.0	A
$I_{Limit}$	Current Limit 5% higher than $[I_{max} + I_{inrush(max)}]$	5.78	A
Selected Value	UVLO, PLIM and Current limit Calculation	Value	Unit
$R3_{sel}$	Power Limiting (PLIM) setting $[0\Omega$ to Disable]	0	$\Omega$
$R2_{sel}$	Voltage Divider UVLO and GND	14.4	k $\Omega$
$R1_{sel}$	Voltage Divider Reference	778	k $\Omega$
$R_{ILIM}$	Current Limit Set Resistor	3.1	k $\Omega$
$C_{dv/dt}$	Current Limit Set Resistor	22	nF
Results	Current Limit Calculation Description	Value	Unit
$UV_{final}$	Under-voltage Lockout Set point	21.5	V
$Power_{fail}$	Power Fail Detection Set Point	20.19	V
$I_{iLim(final)}$	Final Current Limit Set Point	5.83	A
$T_{dv/dt}$ with $I_{inrush(max)}$	Time to power up with inrush limiting	11	ms

Table C.1.: eFuse IC Design Calculations

## C.2. Motor Driver Latch Configuration

The additional reset latch is based on a NAND latch shown in Figure C.2 and holds the motor in the disable state if a fault is detected by the driver such as an under voltage, overcurrent or thermal shutdown event. The  $\overline{RESET}$  is monitored to generate an interrupt when an error occurs. This error can only be cleared by the microcontroller toggling the  $RESET$  line or power cycling the stem to protect the motor and driver.

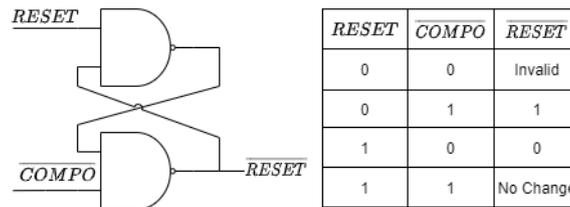


Figure C.2.: Reset Latch

The level at which the overcurrent fault is triggered can be adjusted by setting the reference voltage level of the comparator built into each driver using a voltage divider. This level is then compared with  $COMP_N$  which is the voltage measured using the sense resistor between GND and PGND.

$$I_{trip}(A) = \frac{COMP_P(V)}{R_{sense}(\Omega)} \quad (\text{Eq. C.2.1})$$

where:

- $R_{sense}$  is selected to be  $0.1\Omega$
- $I_{trip}$  is set to 3A
- The result is that 0.3V needs to be set at COMPP
- This voltage is set by dividing the 3.3V supply with  $R_1$   $k\Omega$  and  $R_2$  values of 10 and 1  $k\Omega$  respectively

# D. Expansion Header Pinouts

## D.1. Master Expansion Header

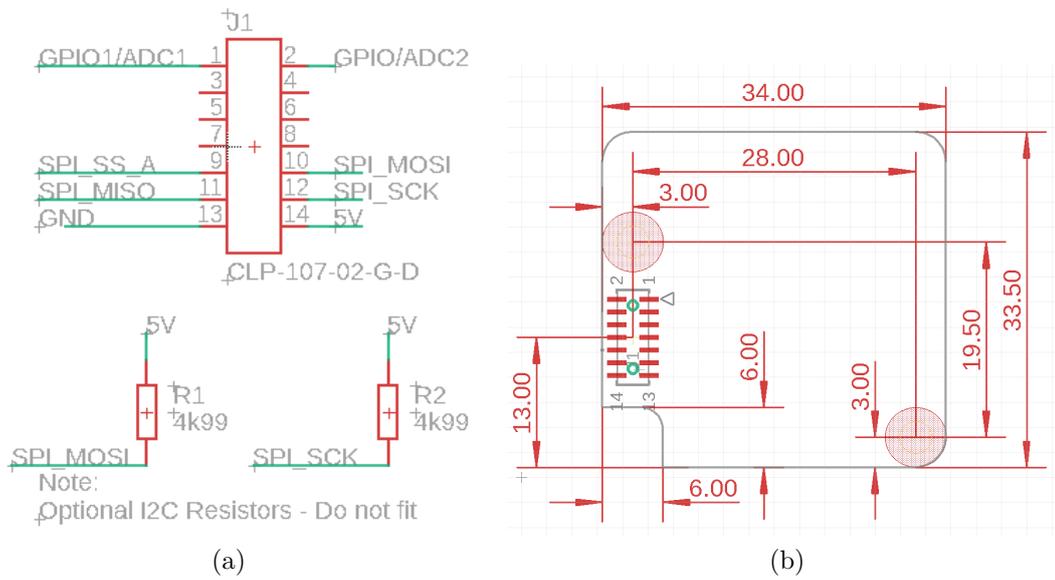


Figure D.1.: (a) Master Expansion Interface pin-out (b) Expansion board dimensions

## D.2. Master Expansion Header

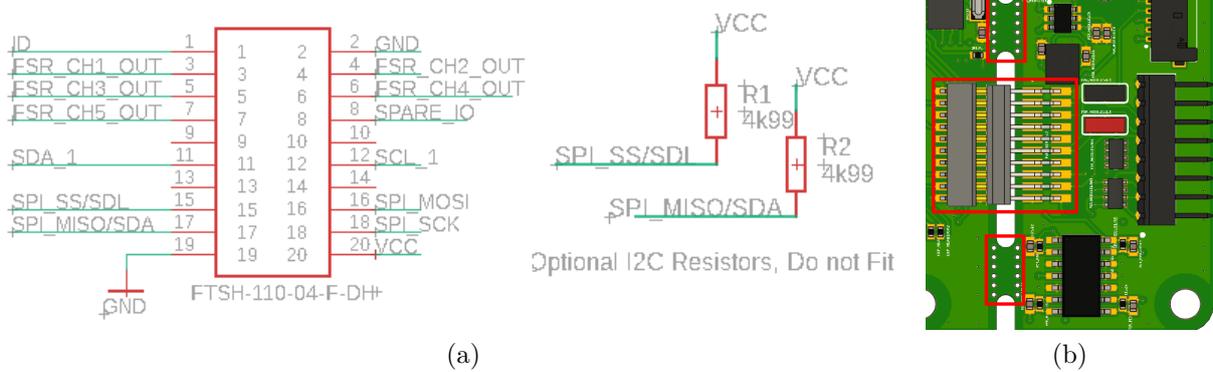


Figure D.2.: (a) Expansion connector pinout (b) Expansion connector and breakaway section

## E. Firmware Configuration Definitions

ADS1299 Configuration The *ADS1299* incorporates all commonly-required features for EMG including on-board reference generation, programmable gain, filtering and simultaneous conversion of up to eight input channels. The internal reference and oscillator were used in favour of providing these externally. Configuration and transfer of the conversion data occurs via the SPI interface. The block diagram for the *ADS1299* is shown in Figure E.1.

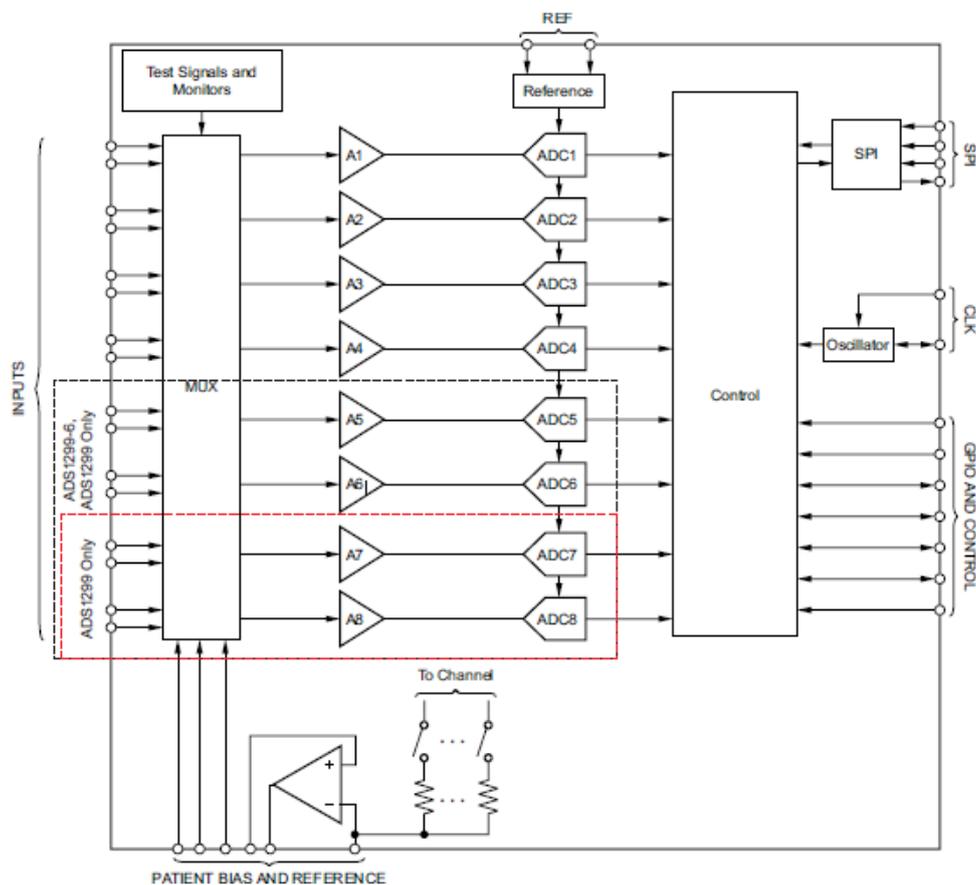


Figure E.1.: ADS1299 Block Diagram [Tex16]

The configuration of the *ADS1299* is done by programming the configuration registers over SPI. The settings configure the signal routing, channel settings and conversion settings. The internal test signal is particularly useful during development to ensure data is acquired correctly by providing a known square wave output. The settings used in this implementation are based on those used in the open source firmware provided by OpenBCI [Ope] which uses the same AFE. These settings have been confirmed to work in an sEMG application and are shown in Table E.1.

Register	Configuration
<b>CONFIG1</b>	
Daisy Chain	Off
Sample Rate	1000 SPS
<b>CONFIG2</b>	
Internal Test Signal	On
Test Signal Amplitude	$V_{REF}/2400$
Test signal Frequency	$f_{clk}/2^{21}$
<b>CONFIG3</b>	
Internal reference	On
Internal Bias Buffer	On
BIAS measurement	Open
<b>LOFF</b>	
Lead Off Detection	Off
<b>CHnSet</b>	
Input Mux	Normal Electrode Input <sup>1</sup>
SRB2	Closed
Gain	24
<b>BIAS_SENSP</b>	
INxP to BIAS	All On (0xff)
<b>BIAS_SENSN</b>	
INxN to BIAS	All On (0xff)
<b>MISC1</b>	
SRB1	All Off (0x00)

<sup>1</sup> Set to internal test signal during development

Table E.1.: ADS1299 Register Configuration

The data protocol for obtaining reading from the *ADS1299* is shown in Figure E.2. Results need to be converted from the unusual 24-Bit format to a more standard 32-Bit two's complement representation and scaled based on the gain setting used.

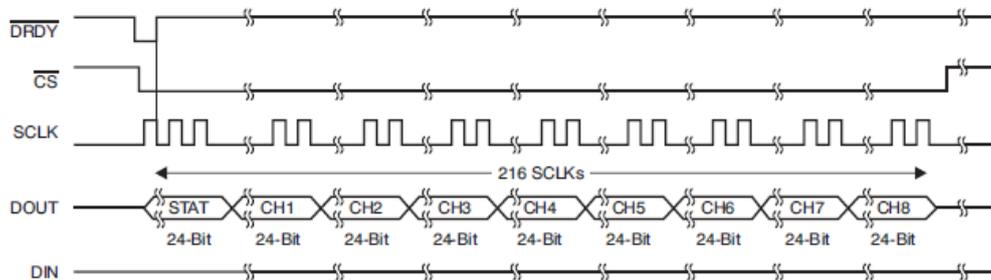


Figure E.2.: ADS1299 data format [Tex16]

## E.1. DMAC Channel Allocation

A summary of the channels used is listed in [Table 4.9](#).

Ch.	Peripheral	Description
<b>Master Board</b>		
0	SERCOM1 <sub>RX</sub>	Master-Slave IF - Transfer Done Event used for CS handling
1	SERCOM5 <sub>RX</sub>	Angle Sensor - Transfer Done Event used for CS handling
2	SERCOM2 <sub>RX</sub>	Expansion IF (EMG) - Transfer Done Event used for CS handling
3	ADC1	Beat Transfer Event Drives CS Pin
4	ADC1	Sequencer - Triggered by TCC0 overflow event
5	SERCOM2 <sub>TX</sub>	Expansion IF (EMG)
6	SERCOM5 <sub>TX</sub>	Angle Sensor
7	SERCOM1 <sub>TX</sub>	Master-Slave IF
<b>Slave Board</b>		
0	SERCOM1 <sub>RX</sub>	Master-Slave IF - Transfer Done Event used for CS handling
1	SERCOM5 <sub>RX</sub>	Angle Sensor - Transfer Done Event used for CS handling
2	ADC0	Result Ready - Triggers Sequencer
3	ADC1	Result Ready - Triggers Sequencer
4	ADC1	Sequencer - Triggered by TCC0 overflow event
5	SERCOM2 <sub>TX</sub>	Expansion IF (EMG)
6	SERCOM5 <sub>TX</sub>	Angle Sensor
7	SERCOM1 <sub>TX</sub>	Master-Slave IF

Table E.2.: DMAC Channel Allocation